ELECTRONICS AND COMMUNICATION ENGINEERING

COIMBATORE INSTITUTE OF TECHNOLOGY

VISION AND MISSION OF THE INSTITUTE

VISION

The Institute strives to inculcate a sound knowledge in engineering along with realized social responsibilities to enable its students to combat the current and impending challenges faced by our country and to extend their expertise to the global arena.

MISSION

The Mission of CIT is to impart high quality education and training to its students to make them world-class engineers with a foresight to the changes and problems and pioneers to offer innovative solutions to benefit the nation and the world at large.

ELECTRONICS AND COMMUNICATION ENGINEERING

COIMBATORE INSTITUTE OF TECHNOLOGY

VISION AND MISSION OF THE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VISION

The Vision of the department is to impart knowledge in the field of Electronics and Communication Engineering so as to nurture excellence in students, mould their capability to meet current and impending challenges and ignite aspirations to become innovators and entrepreneurs, thereby benefit the nation and world.

MISSION

The Mission of Electronics and Communication Engineering Department is

M1 To impart high quality education and training to the students in the field of Electronics and Communication Engineering

M2 To promote creation and dissemination of knowledge.

M3 To provide a framework for innovation and collaborative research with industry.

M4 To equip the graduate students with an attitude for professional career and continuous learning.

ELECTRONICS AND COMMUNICATION ENGINEERING

COIMBATORE INSTITUTE OF TECHNOLOGY

PROGRAMME EDUATIONAL OBJECTIVES (PEOs) OF M.E. VLSI DESIGN

The following Programme Educational Objectives are designed for M.E. VLSI Design programme in Electronics and Communication Engineering based on the Department Mission to provide higher engineering education and motivate research in the field of VLSI Engineering

PEO1 To develop outstanding technical and professional expertise that enables the students to integrate themselves with new developments in VLSI technology for successful career in global, industrial, academic and research domains.

PEO2 To develop communication skills, interpersonal skills, managerial skills, entrepreneurial skills and inculcate ethics and values needed for professional success in national and multinational companies, institutions and organizations.

PEO3 To explore engineering solutions with good ethical standards and professional attitude for significant research in solving contemporary social and human issues within realistic constraints and acquire an aptitude for lifelong learning.

ELECTRONICS AND COMMUNICATION ENGINEERING

COIMBATORE INSTITUTE OF TECHNOLOGY

PROGRAMME OUTCOMES (POs) OF M.E. VLSI DESIGN

Students in the Department of Electronics and Communication Engineering M.E. VLSI Design programme should at the time of their graduation are in possession of :

PO1 an ability to apply knowledge from graduate engineering to present solutions for technical problems in various engineering fields related to VLSI Design and Technology.

PO2 an ability to apply knowledge of VLSI in a creative and innovative way to identify, formulate, design and develop products useful to human society.

PO3 an ability to apply advanced technical knowledge in multiple contexts to solve global and societal contemporary problems.

PO4 an ability to understand and design advanced VLSI based systems, conduct an organized and systematic study on significant research topic within the field of VLSI and its allied field.

PO5 an ability to use modern Electronic Design Automation (EDA) tools, software and hardware essential to interpret, evaluate and analyze the systems in VLSI design environments.

PO6 an ability to conduct and produce quality research in the diversified fields of engineering by applying the knowledge of VLSI systems.

PO7 a skill to exhibit a commitment for professional practices by continuous learning and need for sustainable development in VLSI industry.

PO8 an ability to make professional and ethical decisions with an understanding of the impact of VLSI Technology solutions on societal, economic, global and environmental issues.

PO9 an ability to develop professional skill to function effectively as an individual and as a member or leader in diverse teams that contribute to the success of the organizations.

PO10 self confidence and communication skill to express their knowledge in VLSI engineering, design and prepare documentation.

PO11 an ability to undertake collaborative projects with industries and organizations in multidisciplinary environments.

PO12 an ability to develop confidence for self-education and lifelong learning in the broadest context of technological change.

COIMBATORE INSTITUTE OF TECHNOLOGY

(Government Aided Autonomous Institution Affiliated to Anna University, Chennai)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Curriculum from the Academic Year 2015 - 2016 onwards

Name of the degree : M.E (Full Time)

Specialization : VLSI Design

Semester I

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD11	Graph Theory and Optimization Techniques	4	0	0	4	FC
15MVD12	Advanced Digital System Design	3	0	0	3	PC
15MVD13	CMOS VLSI Design	3	0	0	3	PC
15MVD14	System Design using FPGA	3	0	0	3	PC
15MVD15	Analog VLSI Circuits	3	0	0	3	PC
	Elective-I	3	0	0	3	PE
	PRACTICAL					
15MVD16	VLSI Design Laboratory -I	-	-	4	2	PC
15MVD17	Seminar and Technical Writing	-	-	2	1	EEC
	TOTAL CREDITS				**22**	

Semester II

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD21	Low power CMOS Circuits and Memories	3	0	0	3	PC
15MVD22	Mixed Signal Circuit Design	3	0	0	3	PC
15MVD23	Testing of VLSI Circuits	3	0	0	3	PC
15MVD24	CAD for VLSI Circuits	3	0	0	3	PC
	Elective II	3	0	0	3	PE
	Elective III	3	0	0	3	PE
	PRACTICAL					
15MVD25	VLSI Design Laboratory - II	-	-	4	2	PC
15MVD26	Mini project	-	-	4	2	EEC
	TOTAL CREDITS				**22**	

Semester III

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
	Elective-IV	3	0	0	3	PE
	Elective-V	3	0	0	3	PE
	Elective -VI	3	0	0	3	PE
	PRACTICAL					
15MVD41	Project Work & Viva Voce					EEC
	TOTAL CREDITS				**9**	

Semester IV

Course Code	Course Name	L	T	P	C	CAT
	PRACTICAL					
15MVD41	Project Work & Viva Voce				18	EEC
	TOTAL CREDITS				**18**	
	GRAND TOTAL CREDITS				**71**	

TOTAL CREDITS - 71

Note : L-Lecture, T-Theory, P-Practical, C-Credit

LIST OF PROFESSIONAL ELECTIVES (PE)

Sl.No.	Course Code	Course Name	L	T	P	C	CAT
1.	15MVDE01	Advanced Computer Architecture and Parallel Processing	3	0	0	3	PE
2.	15MVDE02	Semiconductor Device Modelling	3	0	0	3	PE
3.	15MVDE03	Nano Electronics	3	0	0	3	PE
4.	15MVDE04	Signal Integrity for High Speed Devices	3	0	0	3	PE
5.	15MVDE05	High Speed Digital Design	3	0	0	3	PE
6.	15MVDE06	DSP Integrated Circuits	3	0	0	3	PE
7.	15MVDE07	ASIC Design	3	0	0	3	PE
8.	15MVDE08	Microsensors and MEMS	3	0	0	3	PE
9.	15MVDE09	Advanced Embedded System Design	3	0	0	3	PE
10.	15MVDE10	Data Converters	3	0	0	3	PE
11.	15MVDE11	VLSI Technology	3	0	0	3	PE
12.	15MVDE12	Solar Photo Voltaic System	3	0	0	3	PE
13.	15MVDE13	VLSI for Biomedical Applications	3	0	0	3	PE
14.	15MVDE14	Genetic Algorithms for VLSI	3	0	0	3	PE
15.	15MVDE15	Network on Chip	3	0	0	3	PE
16.	15MVDE16	Hardware Software Co-Design	3	0	0	3	PE
17.	15MVDE17	VLSI for Wireless Communication	3	0	0	3	PE
18.	15MVDE18	VLSI Signal Processing	3	0	0	3	PE
19.	15MVDE19	VLSI Architecture for Image and Video Processing	3	0	0	3	PE
20.	15MVDE20	Reconfigurable Architectures	3	0	0	3	PE
21.	15MVDE21	System On Chip	3	0	0	3	PE
22.	15MVDE22	Physical design of VLSI circuits	3	0	0	3	PE
23.	15MVDE23	Artificial Intelligence and Optimization Techniques	3	0	0	3	PE
24.	15MVDE24	Reliability Engineering	3	0	0	3	PE
25.	15MVDE25	Pattern Recognition and Machine Learning	3	0	0	3	PE

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Curriculum from the Academic Year 2015 - 2016 onwards

Name of the degree : M.E (Part Time)

Specialization : VLSI Design

Semester I

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD11	Graph Theory and Optimization Techniques	4	0	0	4	FC
15MVD12	Advanced Digital System Design	3	0	0	3	PC
15MVD13	CMOS VLSI Design	3	0	0	3	PC
	PRACTICAL					
15MVD16	VLSI Design Laboratory - I	-	-	4	2	PC
	TOTAL CREDITS				**12**	

Semester II

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD21	Low power CMOS Circuits and Memories	3	0	0	3	PC
15MVD22	Mixed Signal Circuit Design	3	0	0	3	PC
15MVD23	Testing of VLSI circuits	3	0	0	3	PC
	PRACTICAL					
15MVD25	VLSI Design Laboratory -II	-	-	4	2	PC
	TOTAL CREDITS				**11**	

Semester III

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD14	System Design using FPGA	3	0	0	3	PC
15MVD15	Analog VLSI Circuits	3	0	0	3	PC
	Elective I	3	0	0	3	PE
	PRACTICAL					
15MVD17	Seminar and Technical Writing	-	-	2	1	EEC
	TOTAL CREDITS				**10**	

Semester IV

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
15MVD24	CAD for VLSI Circuits	3	0	0	3	PC
	Elective II	3	0	0	3	PE
	Elective III	3	0	0	3	PE
	PRACTICAL					
15MVD28	Mini project	-	-	4	2	EEC
	TOTAL CREDITS				**11**	

Semester V

Course Code	Course Name	L	T	P	C	CAT
	THEORY					
	Elective IV	3	0	0	3	PE
	Elective V	3	0	0	3	PE
	Elective VI	3	0	0	3	PE
	PRACTICAL					
15MVD41	Project Work & Viva Voce					EEC
	TOTAL CREDITS				**9**	

Semester VI

Course Code	Course Name	L	T	P	C	CAT
	PRACTICAL					
15MVD41	Project Work & Viva Voce				18	EEC
	TOTAL CREDITS				**18**	
	GRAND TOTAL CREDITS				**71**	

Note : L-Lecture, T-Theory, P-Practical, C-Credit

15MVD11 - GRAPH THEORY AND OPTIMIZATION TECHNIQUES

L	T	P	C
4	0	0	4

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will acquire knowledge on fundamentals of graph theory, different graphs and it special classes, physical design algorithms, linear and dynamic programming.

COURSE OUTCOME

Upon completion of this course the students of I year M.E. VLSI Design will be able to demonstrate an ability to

CO1 *: identify and analyze the concepts of graph theory and its special classes.*

CO2 *: analyze different graphical algorithms in physical design of VLSI and apply linear and dynamic programming methods in field of VLSI.*

BASIC CONCEPTS IN GRAPH THEORY

Undirected graph - degree of a vertex - degree sequence - subgraphs - vertex induced subgraphs - complement of a graph - self complementary graphs - walk, path, connectivity, eccentricity, radius, diameter, vertex and edge cuts - vertex partition - independent set - clique. Digraph - orientation - strongly, weakly and unilaterally connected digraphs - directed acyclic graph - adjacency matrix and incidence matrix of graphs - Trees, spanning trees, matrix tree theorem. **(12)**

SPECIAL CLASSES OF GRAPHS

Complete graphs - bipartite graphs - grid graphs - Eulerian graphs - Euler's theorem. Hamiltonian graphs - Dirac's and Ore's theorems - closure of a graph - Bondy-Chvatal theorem - traveling salesman problem - Planar graphs - Euler's formula - Kuratowski's theorem - embedding - dual, five color and four color theorems (without proof) - Overlap graph, containment graph - interval graph - permutation graph - neighborhood graph and rectangular dual - relationship between these graph classes. **(12)**

GRAPH ALGORITHMS IN VLSI PHYSICAL DESIGN

Search algorithms - depth first search and breadth first search - spanning tree algorithms - Kruskal and Prim - shortest path algorithms - Dijkstra and Floyd-Warshall - vertex coloring - Welsh-Powell algorithm - matching, perfect matching, bipartite matching - augmenting path algorithm - min-cut and max-cut algorithms. **(12)**

LINEAR PROGRAMMING

Definition, simplex, two-phase simplex and dual simplex algorithms. **(12)**

DYNAMIC PROGRAMMING

Multistage decision process, computational procedure, final and initial value problems, continuous dynamic programming, discrete dynamic programming **(12)**

TOTAL : 60

REFERENCES

1. *Sherwani N.A, "Algorithms for VLSI Physical Design Automation", Springer-Verlag, 2007.*
2. *Taha H.A, "Operations Research", Prentice Hall, 2003.*
3. *West D.B, "Introduction to Graph Theory", Pearson Education, 2007.*
4. *Yellen J and Gross J, "Graph Theory and its Applications", Chapman & Hall, 2006.*
5. *Gerez S.H, "Algorithms for VLSI Design Automation", John Wiley, 2007.*
6. *Kocay W and Kreher D.L, "Graphs, Algorithms and Optimization", Chapman & Hall, 2005.*
7. *Papadimitriou C.H and Steiglitz K, "Combinatorial Optimization", Prentice Hall, 1997.*

15MVD12 - ADVANCED DIGITAL SYSTEM DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will acquire knowledge on fundamentals of Synchronous and Asynchronous sequential logic circuits, design of system controller using digital circuits, fundamentals of VHDL, SM Chart and floating point arithmetic

COURSE OUTCOME

Upon completion of this course the students of I year M.E. VLSI Design will be able to demonstrate an ability to

CO1 *: identify, design and analyze Synchronous and Asynchronous sequential logic circuits and design and develop system controller*

CO2 *: explain the fundamentals of VHDL, implement of SM Chart and Floating point arithmetic.*

SYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of clocked synchronous sequential circuits - Moore / Mealy State diagrams - State table - State Reduction and Assignment - Design of synchronous sequential circuits. **(9)**

ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN

Analysis of asynchronous sequential circuit - Cycles - Races - Static, Dynamic and Essential hazards - Primitive Flow Table - State Reductions and State Assignment - Design of asynchronous sequential circuits. **(9)**

DESIGN OF SYSTEM CONTROLLER USING COMBINATIONAL AND SEQUENTIAL CIRCUIT

System Controllers - Design Phases - Choosing the controller architecture - State Assignment - Next State decoder - Examples of 2s complement system and Pop Vending Machine - Decoders and Multiplexers in system controllers - Indirect-Addressed MUX configuration - System controllers using ROM, Shift Registers and Counters - General requirements of a programmable controller - Microinstructions - Programmable controllers with fixed instruction set. **(9)**

INTRODUCTION TO VHDL

VHDL Description of Combinational circuits - VHDL Modules - Sequential Statements and VHDL Processes - Modeling Flip-Flops - Processes Using Wait Statements - Transport and Inertial Delays - Data Types and Operators - Modeling Multiplexers, registers and Counters -Behavioral and structural VHDL - Variables, Signals, Constants - Arrays-loops. **(9)**

SM CHARTS AND FLOATING -POINT ARITHMETIC

State Machine Chart - Derivation of SM Charts - Realization of SM Charts - Implementation of the Dice-Game - Microprogramming - Linked state machines - Representation of Floating-Point Numbers - Floating-point Multiplication - Floating-Point Addition - Other Floating-Point Operations. **(9)**

TOTAL : 45

REFERENCES

1. *William I. Fletcher, "An Engineering Approach to Digital Design", Prentice Hall India, 2011.*
2. *Charles H.Roth Jr "Digital Systems Design using VHDL,"Cengage Learning, 2013.*
3. *Nripendra N Biswas "Logic Design Theory" Prentice Hall, 2001.*
4. *Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL", 2nd Edition, Prentice Hall, 2002.*
5. *Mark Zwolinski, "Digital System Design with VHDL, 2nd Edition, Pearson Education, 2000.*
6. *Stephen Brown,Zvonko Vranesic, "Digital system Design Using VHDL",3rd Edition,Tata Mc Graw Hill,2009*

15MVD13 - CMOS VLSI DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year M.E. (VLSI Design) will be able to acquire knowledge on VLSI Design Process, MOS Circuits, CMOS logic structures, sequential logic structures, Timing issues and CMOS Subsystems.

COURSE OUTCOME

Upon the completion of this course, students will be able to demonstrate an ability to

CO1 *: describe VLSI Design Process, analyze and design CMOS logic circuits*

CO2 *: design CMOS sequential logic circuits and arithmetic circuits and analyze the timing issues.*

MOS CIRCUIT DESIGN PROCESS

Overview of VLSI Design Process - MOSFET Enhancement Transistors - MOS Physics - nFET Current-Voltage Equations - CMOS Inverter - DC Characteristics - Switching Characteristics - Dynamic Behavior-Power, Energy and Energy delay - Interconnects. **(9)**

COMBINATIONAL CMOS LOGIC DESIGN

Static CMOS Design- Complementary CMOS- Pass Transistor Logic- Transmission Gate Logic -Dynamic CMOS Design- Signal Integrity Issues. **(9)**

SEQUENTIAL CMOS LOGIC DESIGN

Static Latches and Registers - Dynamic Latches and Registers - Pulse Registers - Sense Amplifier based Registers - Pipelining - Nonbistable Sequential Circuits. **(9)**

TIMING ISSUES IN VLSI CIRCUITS

Timing Classification of Digital Systems - Timing Issues in Synchronous Design - Self Timed Circuit Design - Synchronizers and Arbiters. **(9)**

DESIGN OF ARITHMETIC BUILDING BLOCKS

Datapaths in Digital Processor Architecture - Design of Adders: Binary Adder and Full Adder - Multiplier - Barrel and Logarithmic Shifters - Magnitude and Equality Comparators - Power and Speed Trade-offs in Datapath Structures. **(9)**

TOTAL : 45

REFERENCES

1. *Jan M Rabaey, Anantha Chandrakasan and Borivoje Nikolic, "Digital Integrated Circuits - A Design Perspective", 2nd Edition, Prentice Hall, 2012.*
2. *John P.Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley & Sons, 2012.*

3. *Neil H. E. Weste and Kamran Eshraghian, "Principles of CMOS VLSI Design - A Systems Perspective", 2nd Edition, Pearson Education, 2010.*
4. *Kamran Eshraghian, Douglas A. Pucknell, "Essentials of VLSI Circuits and Systems", Prentice Hall, 2011*
5. *C.Mead and L.Conway, "Introduction to VLSI Systems", Addison Wesley, 1999.*
6. *Kang, "CMOS Digital Integrated Circuits", McGraw Hill, 2002.*

15MVD14 - SYSTEM DESIGN USING FPGA

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of ME (VLSI Design) will be able to acquire knowledge on Hardware Description Languages, Programmable logic devices and FPGAs, design of FPGA based systems, Combinational and sequential networks, FPGA architecture and Large FPGA Systems.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *design digital circuit using HDL and explain the architectures of Programmable logic devices and FPGAs.*

CO2 : *design of FPGA based systems, digital networks, architectures and Large FPGA systems.*

VERILOG HDL FEATURES AND MODELLING

Overview of Digital design with Verilog HDL - Hierarchical Modeling Concepts -Lexical Conventions - Data types - Modules and Ports -Gate Level Modeling: Gate Types - Gate Delays - Data flow Modeling: Continuous Assignments - Expressions - Operator Types - Behavioral Modeling: Structures Procedures- Procedural Assignments - Conditional Statements - Multiway Branching - Loops - Tasks and Functions- Switch level Modeling -Design of combinational, sequential digital circuits using Verilog HDL. **(9)**

COMPLEX PROGRAMMABLE LOGIC DEVICES AND FGPAs

Programmable Logic to ASICs - PROMS, PLAs, PALs, MGA ASICs, CPLDs and FPGAs - CPLDs - CPLD Architectures - Function Blocks - I/O Blocks - Clock Drivers - Interconnects - CPLD Technology and Programmable Elements - Embedded devices.

FPGAs - FPGA Architectures - Configurable Logic Blocks - Configurable I/O Blocks - Programmable interconnects - Clock Circuitry - SRAM vs Antifuse Programming - Emulating and prototyping ASICs.

Comparison of CPLDs and FPGAs. **(9)**

FPGA BASED SYSTEMS AND FABRICS

Introduction - Basic Concepts- Digital Design and FPGAs - Role of FPGAs - FPGA Types - FPGA Based System Design- Registers and RAM.

Introduction to FPGA Fabrics - FPGA Architectures - SRAM Based FPGAs - Permanently Programmed FPGAs-Chip I/O - Circuit Design of FPGA Fabrics - Architecture of FPGA Fabrics. **(9)**

COMBINATIONAL AND SEQUENTIAL LOGIC NETWORKS DESIGN

Logic design Process - Modeling with HDLs - Combinational Network Delay-Power and Energy Optimization - Arithmetic Logic - Logic implementation for FPGAs - Physical Design for FPGAs - Sequential Machine Design Process - Sequential Design styles - Rules for Clocking - Performance analysis - Power Optimization. **(9)**

FPGA ARCHITECTURE DESIGN AND LARGE SCALE SYSTEMS

Behavioral Design - Data path controller Architectures - Scheduling and Allocation - Power - Pipelining - Design Methodologies - Design Example - Digital Signal Processor.

Introduction to Large scale systems - Busses - Platform FPGAs - Multi FPGA systems, Novel Architectures **(9)**

TOTAL : 45

REFERENCES

1. *Samir Palnitkar, "Verilog HDL", 2nd Edition, Pearson Education, 2004.*
2. *Wayne Wolf, "FPGA- based System Design", Pearson Education, International Edition, 2004*
3. *Bob Zeidman, "Designing with FPGAs and CPLDs, Elsevier, CMP Books, 2002.*
4. *Ion Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier, 2008.*
5. *Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Prentice Hall, 2002.*
6. *Charles H.Roth Jr "Digital Systems Design using VHDL", Cengage Learning, 2013.*

15MVD15 - ANALOG VLSI CIRUCITS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will acquire knowledge on CMOS fabrication processes and models, analyze and design analog CMOS sub-circuits, Biasing circuits, Amplifiers and operational amplifiers.

COURSE OUTCOME

Upon completion of this course the students of I year M.E. VLSI Design will be able to demonstrate an ability to

CO1 : *model, analyze and design analog CMOS circuits.*

CO2 : *analyze and design single stage, differential amplifiers, feedback amplifiers and operational amplifiers.*

CMOS TECHNOLOGY AND DEVICE MODELING

Basic MOS semiconductor fabrication processes - other considerations of CMOS technology - MOS I/V characteristics MOS large signal model and parameters - Small signal model for the MOS transistor - Computer simulation models -Sub threshold MOS model. **(9)**

ANALOG CMOS SUB CIRCUITS AND BIASING CIRCUITS

MOS switch - MOS diode and active resistor - Basic Current mirrors - Cascode current mirrors-active current mirrors- voltage references-supply independent biasing, temperature independent references, PTAT current generation. **(9)**

SINGLE STAGE AMPLIFIERS AND DIFFERENTIAL AMPLIFIERS

Common source stage - Common source stage with resistive load - diode connected load - current source load - triode load - source degeneration - Source follower stage - Common -gate stage - Cascade stages -Single ended and differential operation - Basic differential pair - Common mode response - Differential pair with MOS loads. Gilbert Cell. **(9)**

HIGH FREQUENCY AND NOISE CHARACTERISTICS OF AMPLIFIERS

General considerations-Miller effect -Association of poles with Nodes - Frequency response of Common source, Source follower, Common gate amplifiers, Cascode amplifiers and differential amplifiers - Statistical characteristics of noise - Types of Noise - Noise in single stage amplifiers -Noise in differential pairs. **(9)**

FEEDBACK AND OPERATIONAL AMPLIFIERS

Properties of feedback circuits - Feedback Topologies - Effect of loading in feedback networks - Effect of feedback on noise - Performance parameters of operational amplifiers - One stage op amp - Two stage op amp - Gain Boosting - Input range limitations - Slew rate - Power Supply Rejection- Noise in op amps - Stability and Frequency compensation. **(9)**

TOTAL : 45

REFERENCES

1. *Phillip E.Allen and Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.*
2. *Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2001*
3. *Malcom R.Haskard and Lan C.May, "Analog VLSI Design - NMOS and CMOS", Prentice Hall, 1998.*
4. *Randall L Geiger, Phillip E. Allen and Noel K.Strader, "VLSI Design Techniques for Analog and Digital Circuits", Mc Graw Hill International Company, 1990.*
5. *K.Radhakrishna Rao," Electronics for Analog Signal Processing-I", NPTEL, Courseware, 2005.*

15MVD16 - VLSI DESIGN LABORATORY I

L	T	P	C
0	0	4	2

ASSESSMENT : PRACTICAL

COURSE OBJECTIVE

The students of first year M.E (VLSI Design) will be able to acquire knowledge on front end and back end tools in the design of VLSI circuits, design and implement digital circuits using HDL , interface the peripheral boards with FPGAs and performing the RTL Synthesis of CMOS Circuits.

COURSE OUTCOME

Upon the completion of this course, students will be able to demonstrate an ability to

CO1 : *design and simulate the CMOS digital and analog VLSI Circuits using Modern Tools, interface peripheral boards with FPGA, design layout of CMOS Circuits using back end tool and perform RTL synthesis using Xilinx Tool.*

CO2 : *develop skills to communicate effectively.*

LIST OF EXPERIMENTS

1. Writing Test benches using HDL for combinational and sequential circuits
2. Design and simulation of 4-bit barrel shifter using HDL
3. Design and simulation of 4-bit carry save adder using HDL
4. Design and simulation of Booth multiplier using HDL
5. Design and simulation of FSM using HDL
6. RTL Synthesis using Xilinx Tool
7. Design and Implementation of Matrix keyboard/ Stepper Motor controller using VHDL
8. IC Layout Design using EDA Tools (CMOS NOT, NAND & NOR Gates)
9. Design and simulation of differential amplifiers
10. Design and simulation of operational amplifiers

REFERENCES

1. *Neil Weste and Kamran Eshranghian, "Principles of CMOS VLSI Design", Addison Wiley, 2012.*
2. *Etienne Sicard and Sonaia Delmas Bendhia, "Basics of CMOS Cell Design", Tata McGraw Hill Publishing, 2007.*
3. *Etienne Sicard and Sonaia Delmas Bendhia, "Advanced CMOS Cell Design", Tata McGraw Hill Publishing, 2007*
4. *S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley and Sons, 2002.*
5. *N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.*
6. *VLSI Lab Manual, prepared by Department of Electronics and Communication Engineering, CIT.*

15MVD17 - SEMINAR AND TECHNICAL WRITING

L	T	P	C
0	0	2	1

ASSESSMENT : PRACTICAL

COURSE OBJECTIVE

The first year M.E VLSI Design students will acquire practical knowledge to identify, formulate, analyze/ solve basic design problems for human needs with the knowledge of contemporary issues and to work as individual or in teams to develop solutions using electronic hardware and /or software.

COURSE OUTCOME

Upon completion of this course the students will be able to demonstrate an ability to

CO1 **:** *use techniques, skills and modern engineering tools for developing solutions to solve basic problems of societal needs with the knowledge of contemporary issues.*

CO2 **:** *develop skills to communicate effectively.*

15MVD21 - LOW POWER CMOS CIRCUITS AND MEMORIES

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will acquire knowledge on basics of low power VLSI design and its power analysis methods, Circuit and logic level low power design of VLSI Circuits, Power dissipation in clock distribution, Memories and its advanced technologies, reliability issues on Memories.

COURSE OUTCOME

Upon completion of this course the students will be able to demonstrate an ability to

CO1 : *illustrate the low power analysis of VLSI Circuits using various methods, design the logic and circuit level low power circuits and impact of power on clock distribution.*

CO2 : *exemplify the basic and advanced memory technologies, types of memories and its reliability issues.*

INTRODUCTION TO LOW POWER VLSI DESIGN AND POWER ANALYSIS METHODS

Need for low power VLSI chips - Sources of power dissipation on Digital Integrated circuits - Physics of power dissipation in CMOS devices - Dynamic dissipation in CMOS - Technology impact on Low power- SPICE circuit simulators - Gate level logic simulation - Capacitive power estimation - Static state power - Gate level capacitance estimation. **(9)**

CIRCUIT AND LOGIC LEVEL LOW POWER DESIGN AND CLOCK DISTRIBUTION

Circuit level: Power consumption in circuits - Flip Flops and Latches design - High capacitance nodes - Low power digital cells library - Logic level: Gate reorganization - signal gating - logic encoding - state machine encoding - pre-computation logic.

Power dissipation in clock distribution - Single driver Vs Distributed buffers - Zero skew Vs tolerable skew - Chip and package co-design of clock network. **(9)**

RANDOM ACCESS MEMORY TECHNOLOGIES

SRAM cell structures - MOS SRAM Architecture and peripheral Circuit Operation - Advanced SRAM Architectures and Technologies - DRAM - CMOS DRAM - DRAM cell structures - BiCMOS DRAM - soft error failures in DRAM - Advanced DRAM Design and Architecture - Application Specific SRAMs and DRAMs. **(9)**

NON-VOLATILE MEMORIES

Masked ROMs - High Density ROMs - CMOS Programmable EPROMs - Floating Gate and One time Programmable ROMs - Electrically Erasable PROMS - Non volatile SRAM - Flash Memories - Advanced Flash Memory Architecture. **(9)**

ADVANCED MEMORY TECHNOLOGIES AND ITS RELIABILITY ISSUES

Ferroelectric Random Access Memories (FRAMs) - Gallium Arsenide (GaAs) FRAMs - Analog Memories - Magnetoresistive Random Access Memories (MRAMs) - Memory Cards.

Reliability Issues: RAM Failure Modes and Mechanism - Nonvolatile Memory - Modeling and Failure Rate Prediction - Design for Reliability - Test Structures-Screening and Qualification. **(9)**

TOTAL : 45

REFERENCES

1. *Gary K. Yeap ,Farid N. Najm, "Low power VLSI design and Technology", World Scientific Publishing Ltd., 1996.*
2. *Dimitrios Soudris, Christian Piguet, Costas Goutis, "Designing CMOS Circuits for Low Power", Kluwer Academic Publishers,2002.*
3. *Kaushik Roy , Sharat C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley- Interscience, 2000.*
4. *Ashok K Sharma, "Semiconductor Memories Technology, Testing and Reliability", Wiley, 2002.*
5. *Ashok K Sharma, "Advanced Semiconductor Memories - Architecture, Design and Applications, Wiley, 2002.*
6. *Etienne Sicard and Sonaia Delmas Bendhia, "Advanced CMOS Cell Design", Tata McGraw Hill Publishing, 2007.*
7. *Betty Prince, "Emerging Memories: Technologies and Trends", Kluwer Academic publishers, 2002*

15MVD22 - MIXED SIGNAL CIRCUIT DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The first year students of M.E. (VLSI Design) will acquire knowledge on Submicron CMOS circuit design, continuous time filters , switched capacitor circuits, data converters, oscillators and PLL.

COURSE OUTCOME

Upon completion of this course the students will be able to demonstrate ability to

CO1 : *analyze and design submicron CMOS circuits and continuous time filters*

CO2 : *analyze and design switched capacitor circuits, digital to analog converters and analog to digital converters, oscillators and PLLs.*

SUBMICRON CMOS CIRCUIT DESIGN

CMOS Process flow - Capacitors and resistors -Digital circuit design: MOSFET switch - Delay elements - adder- Analog circuit design: Biasing - Op amp Design - Mixed-Signal Layout Issues: Floor Planning- Power Supply and Grounding Issues- Fully Differential Design- Guard Rings- Shielding -Interconnect. **(9)**

CONTINUOUS TIME FILTERS

First order filters-Second order filters- Gm-C filters- Transconductors Using Fixed Resistors- CMOS Transconductors Using Triode Transistors- CMOS Transconductors Using Active Transistors- Bipolar Transconductors - Bicmos Transconductors - Active RC And MOSFET-C Filters- Tuning Circuitry-Complex Filters. **(9)**

NONLINEARITY AND SWITCHED CAPACITOR CIRCUITS

Basic building blocks - Basic operation and analysis - Noise in Switched Capacitor Circuits - First-Order Filters - Biquad Filters- Charge Injection- Switched Capacitor Gain Circuits- Correlated Double-Sampling Techniques- Switched capacitor amplifiers - Switched capacitor integrator - Nonlinearity - Mismatch **(9)**

DIGITAL TO ANALOG AND ANALOG TO DIGITAL CONVERTERS

Introduction and characterization of DAC - Parallel DAC - Extending the resolution of parallel DAC - Serial DAC - Introduction and characterization of ADC - Serial ADC - Medium ADC - High speed ADC. **(9)**

OSCILLATORS AND PLLs

Oscillatory system - Ring oscillators - LC oscillators - Voltage Controlled Oscillators (VCO) -Mathematical model of VCO - Simple PLL - Charge pump PLLs - Non ideal effects in PLLs: PFD/CP non idealities - jitter in PLLs - Delay locked loops - PLL applications. **(9)**

TOTAL : 45

REFERENCES

1. *B. Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2002.*
2. *R.J. Baker, "CMOS Mixed-Signal Circuit Design", Wiley Publications, 2002.*
3. *R.J. Baker, H.W. Li, D.E. Boyce, "CMOS Circuit design, Layout, and Simulation", Wiley-IEEE Press, 3rd Edition, 2010.*
4. *Tony Chan Carusone, David A. Johns and Ken Martin, "Analog Integrated Circuit Design", John Wiley and Sons, 2nd Edition, 2011.*
5. *Phillip E.Allen and Douglas R.Holberg, "CMOS Analog Circuit Design", Oxford University Press, 2002.*

15MVD23 - TESTING OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will acquire knowledge on testing & validation process and analyze faults.

COURSE OUTCOME

Upon completion of this course the students will be able to demonstrate an ability to

CO1 : *generate test patterns for combinational and sequential circuits*

CO2 : *explain about design for testability, Apply testing algorithms to digital circuits and perform fault diagnosis.*

BASICS OF TESTING AND FAULT MODELING

Introduction to Testing - Faults in Digital Circuits - Modeling of faults - Logical Fault Models - Fault detection - Fault Location - Fault dominance - Logic simulation - Types of simulation - Delay models - Gate Level Event-driven simulation. **(9)**

TEST GENERATION FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS

Test generation for Combinational logic circuits - Testable Combinational logic circuit design - Test generation for Sequential circuits - Design of Testable sequential circuits **(9)**

DESIGN FOR TESTABILITY

Design for Testability - Ad-hoc design - Generic Scan based design - Classical scan based design - System level DFT approaches. **(9)**

SELF - TEST AND TEST ALGORITHMS

Built-in self Test - Test pattern generation for BIST - Circular BIST - BIST Architectures - Testable Memory Design - Test Algorithms - Test generation for Embedded RAMs. **(9)**

FAULT DIAGNOSIS

Logical Level Diagnosis - Diagnosis by Unit Under Test reduction - Fault Diagnosis for Combinational Circuits - Self checking design - System level Diagnosis. **(9)**

TOTAL : 45

REFERENCES

1. *M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.*
2. *P.K. Lala, "Digital Circuit Testing and Testability", Academic Press, 2002.*
3. *M.L.Bushnell ,V.D.Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2002.*
4. *A.L.Crouch, "Design Test for Digital IC's and Embedded Core Systems", Prentice Hall International, 2002.*

15MVD24 - CAD FOR VLSI CIRCUITS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of first year ME (VLSI Design) will be able to acquire knowledge on basics of VLSI Design methodologies and VLSI design automation tools, principles of physical design in VLSI, Simulation and synthesis in High Level design methodologies.

COURSE OUTCOME

Upon completion of this course, students will be able to demonstrate an ability to

CO1 : *outline the VLSI design Methodologies, apply the algorithms for VLSI Automation*

CO2 : *explain and evaluate the various physical design concepts, simulation and high level synthesis issues in CAD of VLSI.*

INTRODUCTION TO VLSI DESIGN METHODOLOGIES

VLSI Design Cycle - Physical Design Cycle - Design Styles and comparison of different Design StylesFabrication of VLSI Circuits. **(9)**

VLSI DESIGN AUTOMATION

VLSI Design Automation Tools - Algorithmic Graph Theory and Computational Complexity - Tractable and Intractable Problems - General Purpose Methods for Combinational Optimization - Back tracking and Branch and Bound - Local Search - Simulated annealing and genetic algorithms. **(9)**

PHYSICAL DESIGN

Layout Compaction - Placement and Partitioning - Circuit Representation - placement algorithms - Partitioning - Floor Planning Concepts - Shape Functions and Floor Planning Sizing - types of local routing problems - Area Routing - Channel Routing - Global Routing. **(9)**

SIMULATION AND SYNTHESIS

Simulation - Gate Level Modelling and Simulation - Switch Level Modelling and Simulation - Combinational Logic Synthesis - Binary Decision Diagrams - Two Level Logic Synthesis. **(9)**

HIGH LEVEL SYNTHESIS

Hardware Models - Internal Representation - Allocation assignment and scheduling - Simple Scheduling Algorithm - Assignment Problem. **(9)**

TOTAL : 45

REFERENCES

1. *S.H.Gerez, "Algorithms for VLSI Design Automation", John Wiley and Sons, 2002.*
2. *N.A.Sherwani, "Algorithms for VLSI Physical Design Automation", Kluwar Academic Publishers, 2002.*
3. *Drechsler,R., "Evolutionary Algorithms for VLSI CAD", Kluwer Academic Publishers,Boston, 1998.*
4. *Hill,D.D.Shugard, J. Fishburn and K. Kuetzer, "Algorithms and Techniques for VLSI Layout Synthesis", Kluwer Accademic Publishers, Boston, 1989.*

15MVD25 - VLSI DESIGN LABORATORY II

L	T	P	C
0	0	4	2

ASSESSMENT : PRACTICAL

COURSE OBJECTIVE

The students of first year ME VLSI Design will be able to acquire knowledge on Power analysis for CMOS Circuits, designing analog filters, simulating fault and event driven combinational circuits, designing digital CMOS circuits and memories using backend tool interconnects in VLSI Circuits.

COURSE OUTCOME

Upon the completion of this course, students will be able to demonstrate ability to

CO1 : *perform power analysis, simulate the Memories using HDL and EDA Tools, design filters, simulate the CMOS Circuits in back end and analyze the interconnect issues in VLSI Circuits.*

CO2 : *develop skills to communicate effectively.*

LIST OF EXPERIMENTS

1. Design and simulation of ADC
2. Power analysis of Digital Circuits using HDL
3. Design and Simulation of ROM and RAM model using HDL
4. Design and Simulation of analog filters using Cadence
5. Fault Simulation and Fault Diagnosis of digital circuits
6. Event Driven Simulation for gate level combinational circuits
7. Design and Simulation of CMOS Digital Circuits using EDA tools
8. Design and Simulation of SRAM and DRAM using EDA Tools
9. Implementation of Task Scheduling and Placement Algorithms
10. Interconnects in VLSI circuits

REFERENCES

1. *Kaushik Roy, Sharat C. Prasad, "Low-Power CMOS VLSI Circuit Design", Wiley- Interscience, 2000.*
2. *Ashok K Sharma, "Semiconductor Memories Technology, Testing and Reliability", Wiley, 2002.*
3. *M.Abramovici, M.A.Breuer and A.D. Friedman, "Digital systems and Testable Design", Jaico Publishing House, 2002.*
4. *Etienne Sicard, Sonia Delmas Bendhia," Basics of CMOS Cell Design",Tata Mc Graw Hill Professional, CMOS Circuit Design series,2005.*
5. *VLSI Lab Manual, prepared by Department of Electronics and Communication Engineering, CIT.*

15MVDE01 - ADVANCED COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of MEVLSI Design will be able to acquire knowledge on parallel processing mechanisms, hierarchy of memory structure, memory allocation , memory management, principles of pipelining and vector processing, parallel algorithms for array processors, multiprocessor issues and measuring its performance.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain architectures for parallel processing, memory allocation in cache memories and relate I/O subsystems.*

CO2 : *report on array processing, multi processing and analyze the principles of parallel algorithm design using performance measures.*

PARALLEL PROCESSING, MEMORY AND I/O SUBSYSTEMS

Generation of computer systems - Trends towards parallel processing - Parallel processing mechanisms - Parallel computer structure - Architectural classification schemes - Hierarchical Memory structure - Virtual memory system - Cache memory management - Memory allocation and management - I/O subsystems. **(10)**

PIPELINING AND VECTOR PROCESSING

Principles - Classification of pipeline processors - Reservation tables - Interleaved memory organization - Design of arithmetic pipeline - Design of instruction pipeline - Basic vector processing architecture - Issues in vector processing - Vectorization and optimization methods. **(9)**

ARRAY PROCESSING

SIMD Array processors - SIMD interconnection networks - Parallel algorithms for array processors - Associative array processing. **(8)**

MULTIPROCESSOR ARCHITECTURE

Functional structures - Interconnection network - Multi cache problems and solutions - Exploiting concurrency for multiprocessing. **(9)**

PRINCIPLES OF PARALLEL ALGORITHM DESIGN

Design approaches - Design issues-Performance measures and analysis - Complexities - Anomalies in parallel algorithms - Pseudo code conventions for parallel algorithms - Comparison of SIMD and MIMD algorithms. **(9)**

TOTAL : 45

REFERENCES

1. *Kai Hwang, "Advanced Computer Architecture: Parallelism, Scalability and Programmability", Tata McGraw Hill, 1992.*
2. *Seyed Roosta "Parallel Processing and Parallel Algorithms", Springer Series, 1999.*
3. *John L Hennessy "Computer Architecture a Quantitative Approach", Harcourt Asia Pvt. Ltd., 1999.*
4. *John L Hennessy and David A Patterson "Computer Architecture a Quantitative Approach", Morgan Kaufmann, 4th Edition, Elsevier, 2006*

15MVDE02 - SEMICONDUCTOR DEVICE MODELLING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on quantum mechanics, relate the model parameters to the structure of the devices, behavior of integrated diodes, BJTs and MOSFETs, modeling techniques and mathematical equations for device simulations.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *model the integrated diode and BJT using device equations and by applying SPICE modeling*

CO2 : *model MOSFETs and apply modeling techniques for network equations to analyze the convergence and stability and use mathematical techniques for device simulations.*

INTRODUCTION TO SEMICONDUCTOR PHYSICS & INTEGRATED PASSIVE DEVICES

Review of Quantum Mechanics, Boltzman transport equation. Continuity equation, Poisson equation. Types and Structures of resistors and capacitors in monolithic technology - dependence of model parameters on structure. **(9)**

INTEGRATED DIODES AND BIPOLAR TRANSISTOR

Junction and Schottky diodes in monolithic technologies - static and dynamic behavior - small and large signal models - SPICE models. **(9)**

INTEGRATED MOS TRANSISTOR

nMOS and pMOS Transistor - Threshold voltage - Threshold voltage equations - MOS device equations - Basic DC equations Second order effects - MOS models - Small signal AC Characteristics - MOSFET SPICE model level 1,2,3 and 4. **(9)**

DEVICE MODELLING

Prime importance of circuit and device simulations in VLSI - Nodal, mesh, modified nodal and hybrid analysis equations - Solution of network equations - Sparse matrix techniques - solution of nonlinear networks through Newton-Raphson technique - convergence and stability. **(9)**

MATHEMATICAL TECHNIQUES FOR DEVICE SIMULATIONS

Poisson equation - continuity equation - drift-diffusion equation - Schrodinger equation - hydrodynamic equations - trap rate, finite difference solutions to these equations in 1D and 2D space - grid generation. **(9)**

TOTAL : 45

REFERENCES

1. *Sze S M, "Physics of Semiconductor Devices", 2nd Edition McGraw Hill, New York, 1981.*
2. *Tyagi M S, "Introduction to Semi-conductor Materials and Devices", John Wiley ,2003.*
3. *Tor A Fijedly, "Introduction to Device Modeling and Circuit Simulation", Wiley-Interscience, 1997.*
4. *Arora, N, "MOSFET Models for VLSI Circuit Simulation", Springer-Verlag, 1993.*
5. *Selberherr.S, "Analysis and Simulation of Semiconductor Devices", Springer-Verlag., 1984.*
6. *Grasser,T., "Advanced Device Modeling and Simulation", World Scientific Publishing Company, 2003.*
7. *Trond Ytterdal, Yuhua Cheng and Tor A. Fjeldly Wayne Wolf, "Device Modeling for Analog and RF CMOS Circuit Design", John Wiley & Sons Ltd., 2003.*

15MVDE03 - NANO ELECTRONICS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on nano device fabrication technology, nano structures, nano devices, using nano technology for memory devices and applications of nano electronics in data transmission and interfacing displays.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain principles of nano device fabrication technology and Nano Structures.*

CO2 : *describe the concepts of nano devices, use nano devices for memories and identify new areas of nano device application like Data Transmission and Interfacing Displays.*

TECHNOLOGY AND ANALYSIS

Fundamentals : Dielectric, Ferroelectric and Optical properties - Film Deposition Methods - Lithography- Material removing techniques - Etching and Chemical Mechanical Polishing - Scanning Probe Techniques. **(9)**

CARBON NANO STRUCTURES

Principles and concepts of Carbon Nano tubes - Fabrication - Electrical, Mechanical and Vibration Properties - Applications of Carbon Nano tubes. **(9)**

LOGIC DEVICES

Silicon MOSFET's : Novel materials and alternative concepts - Single electron devices for logic applications - Super conductor digital electronics - Carbon Nano tubes for data processing. **(9)**

MEMORY DEVICES AND MASS STORAGE DEVICES

Flash memories - Capacitor based Random Access Memories - Magnetic Random Access Memories - Information storage based on phase change materials - Resistive Random Access Memories - Holographic Data storage. **(9)**

DATA TRANSMISSION AND INTERFACING DISPLAYS

Photonic Networks - RF and Microwave Communication System - Liquid Crystal Displays - Organic Light emitting diodes. **(9)**

TOTAL : 45

REFERENCES

1. *Rainer Waser, "Nano Electronics and Information Technology, Advanced Electronic materials and novel devices", 3rd Edition, Wiley VCH, 2012.*
2. *T. Pradeep, "Nano: The essentials", Tata McGraw Hill, 2007.*
3. *Charles Poole, "Introduction to Nano Technology", Wiley Interscience, 2003.*
4. *Vladimir V.Mitin, Viatcheslav A. Kochelap, Michael A. Stroscio, "Introduction to Nano Electronics Science, Nanotechnology, Engineering and Applications", Cambridge University Press, 2011.*
5. *C.Wasshuber Simon, "Simulation of Nano Structures Computational Single-Electronics", Springer, 2001.*
6. *Mark Reed and Takhee Lee, "Molecular Nano Electronics, American Scientific Publisher, California", 2003.*

15MVDE04 - SIGNAL INTEGRITY FOR HIGH SPEED DEVICES

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on fundamentals of electromagnetics for signal integrity, its importance for high speed applications, the factors that affect signal integrity, characteristics of dielectric materials, differential signaling and modeling of transmission lines for high speed devices.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate ability to

CO1 : *define the concept of signal integrity using electromagnetic theory, vector functions and explain crosstalk that affect the integration.*

CO2 : *explain the properties of dielectric materials analyze differential signaling and report a physical model for transmission lines.*

SIGNAL INTEGRITY

The importance of signal integrity - new realm of bus design - Electromagnetic fundamentals for signal integrity - Maxwell equations common vector operators - wave propagations - Electrostatics - magneto statics - Power flow and the poynting vector - Reflections of electromagnetic waves. **(9)**

CROSS TALK

Introduction - mutual inductance and capacitance-coupled wave equation - coupled line analysis - modal analysis - cross talk minimization signal propagation in unbounded conductive media - classic conductor model for transmission model. **(9)**

DI-ELECTRIC MATERIALS

Polarization of Dielectric - Classification of Dielectric material - frequency dependent dielectric material - Classification of Dielectric material fiber - Weave effect - Environmental variation in dielectric behavior Transmission line parameters for loose dielectric and realistic conductors. **(9)**

DIFFERENTIAL SIGNALING

Removal of common mode noise - Differential Cross talk - Virtual reference plane-Propagation of model voltages common terminology - drawbacks of differential signaling. **(9)**

PHYSICAL TRANSMISSION LINE MODEL

Introduction - non ideal return paths - Vias - IO design consideration - Push-pull transmitter - CMOS receivers - ESSD protection circuits - On chip Termination. **(9)**

TOTAL : 45

REFERENCES

1. *Stephen H. Hall, Howard L. Heck, "Advanced Signal Integrity for High-Speed Digital Designs", Wiley IEEE Press, 2009.*
2. *James Edgar Buchanan, "Signal and power integrity in digital systems: TTL, CMOS, and BiCMOS ", Mc Graw Hill,1996.*
3. *Greg Edlund, "Timing Analysis and Simulation for Signal Integrity Engineers", Prentice Hall of India, 2008.*
4. *Stephen C. Thierauf, "Understanding Signal Integrity", Pages displayed by permission Artech Publishing House, 2011.*
5. *Eric Bogatin, "Signal and Power Integrity - Simplified", 2nd Edition, Prentice Hall of India, 2010.*
6. *Mike Peng Li, "Jitter, Noise and Signal Integrity at High-Speed", Prentice Hall of India, 2008.*

15MVDE05 - HIGH SPEED DIGITAL DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will acquire knowledge on design of high speed VLSI circuits.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 *: explain Transmission line characteristics and power distribution.*

CO2 *: explain about clock distribution, timing issues, interconnects, EMC and grounding factors.*

TRANSMISSION LINES AND CROSSTALK

Transmission line structures, signal propagation, transmission line parameters, line impedance, propagation delay, Transmission line reflections, Cross talk- Mutual inductance, Mutual capacitance, cross talk induced noise, minimizing cross talk. **(10)**

POWER DISTRIBUTION

Losses, the need for low-impedance planes and decoupling capacitors and their selection. **(9)**

CLOCK DISTRIBUTION AND TIMING

High-quality clock signals to components - boards and systems - Common clock timing and source synchronous timing. **(9)**

INTERCONNECTS & ELECTROMAGNETIC COMPATIBILITY (EMC)

Interconnect technologies - Multilevel multilayer interconnects - propagation delay - crosstalk analysis - Designing for EMC - EMC regulations - typical noise path - methods of noise coupling - methods of reducing interference in systems. **(9)**

GROUNDING

Safety grounds ,signal grounds, single-point ground systems, multi-point ground systems, hybrid grounds, functional ground layout, practical low frequency grounding, hardware grounds, grounding of cable shields, ground loops, shield grounding at high frequencies. **(8)**

TOTAL : 45

REFERENCES

1. *Howard Johnson, Martin Graham, "High speed Digital design", Pearson, 2005.*
2. *Hall S, Hall G and McCall J, "High Speed Digital System Design: A Handbook of Interconnect Theory and Practices", Wiley Interscience,2000*
3. *Hartmut Grabinski, " Interconnects in VLSI design", Kluwer, 2000*
4. *Goel A K , "High speed VLSI interconnections", Wiley 2007*
5. *Bogatin E, "Signal integrity-simplified", Prentice Hall, 2003.*
6. *Paul CR, "Introduction t Electromagnetic compatibility", Wiley 2006.*

15MVDE06 - DSP INTEGRATED CIRCUITS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will acquire knowledge on Fundamentals of digital signal processors, VLSI process technologies, application specific ICs for DSP, signal processing, filter structures, mathematical transformation of the signals, Filter types, factors like sensitivity and noise, signal processing architectures and use of number system in reducing memory size.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *report on the digital signal processor, methods of applying VLSI technology to signal processing and apply transformation techniques to manipulate data suitable for filter designs.*

CO2 : *explain the architectures for signal processing, analyze their performance and number systems suitable for filter designs.*

DSP INTEGARTED CIRCUITS AND VLSI CIRCUIT TECHNOLOGIES

Standard digital signal processors - Application specific IC's for DSP - DSP systems - DSP system design - Integrated circuit design - MOS transistors - MOS logic - VLSI process technologies. **(9)**

DIGITAL SIGNAL PROCESSING

Digital signal processing - Sampling of analog signals - Selection of sample frequency - Signal processing systems - Frequency response - Transfer functions - Signal flow graphs - Filter structures- Adaptive DSP algorithms - DFT - FFT - Image coding - Discrete cosine transforms. **(9)**

DIGITAL FILTERS AND FINITE WORD LENGTH EFFECTS

FIR filters - FIR filter structures - IIR filters - Specifications of IIR filters - Mapping of analog transfer functions - Mapping of analog filter structures - Multirate systems - Interpolation with an integer factor L - Sampling rate change with a ratio L/M - Multirate filters - Finite word length effects - Parasitic oscillations - Scaling of signal levels - Roundoff noise - Measuring round-off noise - Coefficient sensitivity - Sensitivity and noise. **(9)**

DSP ARCHITECTURES AND SYNTHESIS OF DSP ARCHITECTURES

DSP system architectures - Ideal DSP architectures - Multiprocessors and multicomputers - Systolic and Wave front arrays - Shared memory architectures - Mapping of DSP algorithms onto hardware - Implementation based on complex PEs - Shared memory architecture with Bit - serial PEs. **(9)**

NUMBER SYSTEMS - ARITHMETIC UNITS AND INTEGARTED CIRCUIT DESIGN

Conventional number system - Redundant Number system - Residue Number System - Bit-parallel and Bit-Serial arithmetic - Basic shift accumulator - Reducing the memory size - Complex multipliers - Layout of VLSI circuits. **(9)**

TOTAL : 45

REFERENCES

1. *Lars Wanhammer, "DSP Integrated Circuits", Academic press, New York, 1999.*
2. *Barrett Hazeltine, Lars Wanhammar, Christopher Bull, "Appropriate Technology: Tools, Choices and Implications, Academic Publishers, 1999.*
3. *A.V. Oppenheim et.al, "Discrete-time Signal Processing", Pearson Education, 2000.*
4. *Keshab K.Parhi, "VLSI digital Signal Processing Systems design and Implementation", JohnWiley & Sons, 1999.*
5. *Emmanuel C. Ifeachor, Barrie W. Jervis, "Digital Signal Processing, A Practical Approach", 2nd Edition, Prentice Hall, 2001.*
6. *K. Padmanabhan, S. Anandhi, R. Vijayarajeswaran "A Practical Approach to Digital Signal Processing", New Age International, 2001.*

15MVDE07 - ASIC DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of ME VLSI Design will acquire knowledge on principles of ASIC design flow, fundamentals of logic cells and concepts of various programming technology, high level ASIC design synthesis and ASIC Construction.

COURSE OUTCOME

Upon completion of this course the students will be able to demonstrate an ability to

CO1 *: design sequential and combinational logic cells and analyze Programmable ASICs*

CO2 *: explain ASIC interconnects, design software, synthesize and construct ASICs*

FUNDAMENTALS OF ASICs, CMOS LOGIC AND ASIC LIBRARY DESIGN

Types of ASICs - Design flow-CMOS Transistors CMOS Design Rules - Combinational Logic Cell - Sequential Logic cell - Data path Logic Cell -Transistors as Resistors -Transistor Parasitic Capacitance -Logical effort - Library Cell Design-Library Architecture. **(9)**

PROGRAMMABLE ASICs

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA - Altera FLEX - Altera MAX DC and AC inputs and outputs - Clock and Power inputs - Xilinx I/O blocks. **(9)**

PROGRAMMABLE ASIC INTERCONNECT, DESIGN SOFTWARE AND LOW LEVEL DESIGN ENTRY

Actel ACT - Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX - Design Systems - Logic Synthesis - Half gate ASIC - Schematic entry - Low level design language - PLA tools - EDIF-CFI design representation. **(9)**

LOGIC SYNTHESIS - SIMULATION AND TESTING

Verilog and Logic Synthesis -VHDL and Logic Synthesis - Types of Simulation - Boundary Scan Test - Fault simulation - Automatic Test Pattern Generation. **(9)**

ASIC CONSTRUCTION

System partition - FPGA partitioning - Partitioning methods - Floor planning - placement - Physical Design Flow - Global Routing - Detailed Routing - Special Routing - Circuit extraction - DRC **(9)**

TOTAL : 45

REFERENCES

1. *Smith M.J.S.,"Application Specific Integrated Circuits", Addison, Wesley Longman Inc.,1997.*
2. *Farzad Nekoogar and Faranak Nekoogar, "From ASICs to SoCs - A Practical Approach", Prentice Hall, 2003.*
3. *Wayne Wolf, "FPGA-Based System Design", Prentice Hall, 2004.*
4. *Rajsuman R., "System-on-a-Chip Design and Test", Santa Clara, CA, Artech House Publishers, 2000.*
5. *Nekoogar F.,"Timing Verification of Application-Specific Integrated Circuits", Prentice Hall, 1999*

15MVDE08 - MICROSENSORS AND MEMS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on principles of MEMS and Microsystems, materials used for MEMS, micro sensors, engineering mechanics for micro sensors and design micro systems.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain micro system, apply scaling laws to miniaturization and describe the materials that support miniaturization.*

CO2 : *describe about different micro sensors and engineering mechanics for micro systems, and design micro systems.*

MEMS AND MICROSYSTEMS

MEMS and Microsystems - Evaluation of micro fabrication - micro-systems and microelectronics - applications - working principles of Microsystems - micro-sensors - micro actuators - micro accelerometers - Scaling Laws In Miniaturization - scaling in geometry, rigid body dynamics, trimmer force, electrostatic forces, Electromagnetic forces, electricity and fluidic dynamics and heat - conducting and heat convection. **(9)**

MATERIALS FOR MEMS AND MICROSYSTEMS

Substrates and wafers - silicon as a substrate material - Ideal substrates for MEMS - single crystal silicon and wafers crystal structure - mechanical properties of Si, silicon compounds, SiO2, SiC, Si3N4 and polycrystalline Silicon - silicon piezo resistors, gallium arsenide, quartz, piezoelectric crystals - polymers for MEMS - conductive polymers. **(9)**

MICRO SENSORS

Introduction to micro-sensors - biomedical sensors - pressure sensors - thermal sensors - chemical sensors - moptical sensors - micro-actuation - MEMS with micro actuators. **(9)**

ENGINEERING MECHANICS FOR MICROSYSTEMS DESIGN

Static bending of thin plates - circular plates with edge fixed - rectangular plates with all edges fixed and square plates with all edges fixed - Mechanical vibration - resonant vibration - micro accelerometers - design theory of damping coefficients - Thermo mechanics - thermal stresses - Fracture mechanics - stress intensity factors - fracture toughness and interfacial fracture machine. **(9)**

MICROSYSTEM DESIGN

Design considerations - design constraints - selection of materials - manufacturing process - signal transduction - packaging - process design - photolithography - Thin film fabrications - geometry shaping - mechanical design - design of silicon die for micro-pressure sensor. **(9)**

TOTAL : 45

REFERENCES

1. *Tai Ran Hsu, "MEMS & Micro systems Design, Manufacture and Nano scale Engineering" John Wiley and sons, New Jersey, 2nd Edition, 2008*
2. *Chang Liu, "Foundation of MEMS", Pearson Edition, 2nd Edition ,2011*
3. *Stephen Beeby, Graham Ensell, "MEMS, Mechanical Sensors", Artech House Publishers, 2004.*
4. *Wanjun Wang, Steven A. Soper," Bio-MEMS Technologies and Applications", CRC Press, 2007.*
5. *Sergey Edward Lyshevski, "Nano and Micro Electro Mechanical System", CRC Press, 2001.*
6. *Julian W.Gardner Vijay, K.Varadan, "Micro Sensors, MEMS and Smart Devices", John Wiley & Sons, Ltd, 2nd Edition,2001.*

15MVDE09 - ADVANCED EMBEDDED SYSTEM DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on various hardware units for embedded systems, the concepts of RTOS, methods to interface peripheral devices with processor, Memory Devices, interfacing protocols and modeling of several concurrent processes.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *report on embedded hardware, design an embedded system using RTOS and describe peripheral interfaces.*

CO2 : *explain memory operations, analyze interfacing protocols and examine various concurrent process models.*

INTRODUCTION TO EMBEDDED HARDWARE

Terminology - Gates - Timing diagram - Memory - Microprocessor buses - Direct memory access Interrupts - Built interrupts - Interrupts basis - Shared data problems - Interrupt latency - Embedded system evolution trends - Round robin - Round robin with interrupt function - Rescheduling architecture - algorithm. **(9)**

REAL TIME OPERATING SYSTEM

Task and Task states - Task and data - Semaphore and shared data operating system services - Message queues timing functions - Events - Memory management - Interrupt routines in an RTOS environment - Basic design using RTOS. **(9)**

EMBEDDED HARDWARE, SOFTWARE AND PERIPHERALS

Custom single purpose processors: Hardware - Combination Sequence - Processor design - RT level design - optimizing software: Basic Architecture - Operation - Programmers view - Development Environment - ASIP - Processor Design - Peripherals - Timers, counters and watch dog timers - UART - Pulse width modulator - LCD controllers - Key pad controllers - Stepper motor controllers - A/D converters - Real time clock. **(9)**

MEMORY AND INTERFACING

Memory: Memory write ability and storage performance - Memory types - Composing memory Advance RAM interfacing communication basic - Microprocessor interfacing I/O addressing Interrupts - Direct memory access - Arbitration multilevel bus architecture - Serial protocol - Parallel protocols - Wireless protocols - Digital camera example. **(9)**

CONCURRENT PROCESS MODELS AND HARDWARE SOFTWARE CO - DESIGN

Modes of operation - Finite state machines - Models - HCFSL and state charts language - State machine models - Concurrent process model - Concurrent process - Communication among process -

Synchronization among process - Implementation - Data Flow model. Design technology - Automation synthesis - Hardware software co - simulation - IP cores - Design Process Model. **(9)**

TOTAL : 45

REFERENCES

1. *Steve Heath, "Embedded System Design", 2nd Edition, Newnes Publications, 2004.*
2. *Frank Vahid and Tony Gwargie, "Embedded System Design", 3rd Edition ,John Wiley & sons, 2009.*
3. *David E Simon, "An Embedded Software Primer", Pearson Education Asia, 7th Edition, 2009.*
4. *Rajkamal, "Embedded Systems: Architecture, Programming and Design", 2nd Edition, Tata McGraw-Hill, 2008.*
5. *Arnold Berger, "Embedded System Design: An Introduction to Processes, Tools, and Techniques", CMP Books, 1st Edition, 2002.*

15MVDE10 - DATA CONVERTERS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on sample and hold circuit architecture, switched capacitor circuits and comparators, A/D and D/A converter architectures and precision techniques for obtaining ideal data conversion.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *design sample and hold circuits, switched capacitor circuits and analyze different types of comparator circuits*

CO2 : *design D/A and A/D Converters and apply precision techniques to obtain accurate data conversion.*

SAMPLE AND HOLD CIRCUITS

Sampling switches, Conventional open loop and closed loop sample and hold architecture, Open loop architecture with miller compensation, multiplexed input architectures, recycling architecture switched capacitor architecture. **(9)**

SWITCHED CAPACITOR CIRCUITS AND COMPARATORS

Switched capacitor amplifiers, switched capacitor integrator, switched capacitor common mode feedback. Single stage amplifier as comparator, cascaded amplifier stages as comparator, latched comparators. **(9)**

DIGITAL TO ANALOG CONVERTERS

Performance metrics, reference multiplication and division, switching and logic functions in DAC, Resistor ladder DAC architecture, current steering DAC architecture. **(9)**

ANALOG TO DIGITAL CONVERTERS

Performance metric, Flash architecture, Pipelined Architecture, Successive approximation architecture, Time interleaved architecture. **(9)**

PRECISION TECHNIQUES

Comparator offset cancellation, Op Amp offset cancellation, Calibration techniques, range overlap and digital correction. **(9)**

TOTAL : 45

REFERENCES

1. *Behzad Razavi, "Principles of data conversion system design", IEEE Press, 1995.*
2. *Walter Allan Kester, "The Data Conversion Hand Book", Analog Devices Inc., 2005.*
3. *Behzad Razavi, "Design of Analog CMOS Integrated Circuits", Tata McGraw Hill, 2008.*
4. *Franco Malobert, "Data Converters" Springer Publications, 2007.*
5. *Arthur van Roermund, Herman Casier, Michiel Steyae, "Analog Circuit Design: Smart Data Converters, Filters on Chip, Multimode Transmitters", Springer Publications, 2010.*
6. *Mikael Gustavsson, J. Jacob Wikner, Nianxiong Tan, "CMOS Data Converters for Communications", Kluwer Academic Publishers, 2002.*

15MVDE11 - VLSI TECHNOLOGY

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on Crystal structure, process of crystal growth, properties of materials used for crystal and methods of adding impurities to the base crystal depending on the amount to be doped, device implantation on the crystal using various processing and examine the technique suitable for specific applications.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *describe the suitable crystal structure for VLSI devices,crystal growth conditions and suitable method used for particular impurity doping.*

CO2 : *explain the Building layers of IC using various processing like diffusion, metalization, oxidation, epitaxy, etching lithography and fabrication of devices and circuits.*

MATERIAL PROPERTIES & CRYSTAL GROWTH

Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing consideration, Vapour phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon, Oxidation induced Defects. **(9)**

LITHOGRAPHY AND RELATIVE PLASMA ETCHING

Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, relative Plasma Etching techniques and Equipments.**(9)**

DEPOSITION, DIFFUSION AND METALISATION

Deposition process, Polysilicon, plasma assisted Deposition, Models of Diffusion in Solids, Flick's one dimensional Diffusion Equation - Atomic Diffusion Mechanism - Measurement techniques - Range theory- Implant equipment. Annealing Shallow junction - High energy implantation - Physical vapour deposition - Patterning. **(9)**

PROCESS SIMULATION AND VLSI PROCESS INTEGRATION

Ion implantation - Diffusion and oxidation - Epitaxy - Lithography - Etching and Deposition- NMOS IC Technology - CMOS IC Technology - MOS Memory IC technology - Bipolar IC Technology - IC Fabrication. **(9)**

ASSEMBLY TECHNIQUES AND PACKAGING OF VLSI DEVICES

Analytical Beams - Beams Specimen interactions - Chemical methods - Package types - banking design consideration - VLSI assembly technology - Package fabrication technology. **(9)**

TOTAL : 45

REFERENCES

1. *S.M.Sze, "VLSI Technology", Mc.Graw.Hill Second Edition. 2002.*
2. *Douglas A. Pucknell and Kamran Eshraghian, " Basic VLSI Design", Prentice Hall India, 2003.*
3. *Amar Mukherjee, "Introduction to NMOS and CMOS VLSI System design Prentice Hall India,2000.*
4. *Wayne Wolf ,"Modern VLSI Design", Prentice Hall India,1998.*

15MVDE12 - SOLAR PHOTO VOLTAIC SYSTEM

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on Fundamentals of solar cell, energy conversions, Photovoltaic modules, manufacturing process of solar cells, design of PV systems and its application in socio-economic and environment systems.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain the energy conversion methodologies, structure of the solar cells and photo voltaic modules.*

CO2 : *describe the manufacturing process of PV cells, design of PV systems and demonstrate on its real time applications.*

SOLAR CELL FUNDAMENTALS

Photovoltaic effect - Principle of direct solar energy conversion into electricity in a solar cell. Semiconductor properties, energy levels, basic equations of Solar cell p-n junction structure. **(9)**

PV MODULE PERFORMANCE

I-V characteristics of a PV module, maximum power point, cell efficiency, fill factor, effect of irradiation and temperature. **(9)**

MANUFACTURING OF PV CELLS & DESIGN OF PV SYSTEMS

Commercial solar cells - Production process of single crystalline silicon cells, multi crystalline silicon cells, amorphous silicon, cadmium telluride, copper indium gallium di selenide cells. Design of solar PV systems and cost estimation. Case study of design of solar PV lantern, stand alone PV system - Home lighting and other appliances, solar water pumping systems. **(9)**

CLASSIFICATION OF PV SYSTEMS AND COMPONENTS

Classification - Central Power Station System, Distributed PV System, Standalone PV system, grid Interactive PV System, small system for consumer applications, hybrid solar PV system, concentrator solar photovoltaic. System components - PV arrays, inverters, batteries, charge controls, net power meters - PV array installation, operation, costs, reliability. **(9)**

PV SYSTEM APPLICATIONS

Building - integrated photovoltaic units, grid-interacting central power stations, stand-alone devices for distributed power supply in remote and rural areas, solar cars, aircraft, space solar power satellites - Socio-economic and environmental merits of photovoltaic systems. **(9)**

TOTAL : 45

REFERENCES

1. *Chetan Singh Solanki., Solar Photovoltaic: "Fundamentals, Technologies and Application", Prentice Hall, 2009.*
2. *Jha A.R., "Solar Cell Technology and Applications", CRC Press, 2009*
3. *John R. Balfour, Michael L. Shaw, Sharlave Jarosek., "Introduction to Photo - Voltaic systems", Jones & Bartlett Publishers, Burlington, 2013*
4. *Luque A. L. and Andreev V.M., "Concentrator Photovoltaic", Springer, 2007.*
5. *Partain L.D., Fraas L.M., "Solar Cells and Their Applications", Wiley, 2nd edition, 2010.*
6. *S.P. Sukhatme, J.K.Nayak., "Solar Energy", Tata McGraw Hill, New Delhi, 3rd Edition 2008*

15MVDE13 - VLSI FOR BIOMEDICAL APPLICATIONS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on design of ultra low power VLSI circuits and systems for biomedical applications.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain the concepts of low power analog bio-medical circuits and systems.*

CO2 : *explain about biomedical electronic systems, ultra low power analog and digital circuits and bio-inspired systems.*

LOW-POWER ANALOG BIOMEDICAL CIRCUITS

Low power transimpedance amplifiers and photoreceptors - Low power transconductance amplifiers and scaling laws for power in analog circuits - Low-power filters and resonators - Low power current - mode circuits - Ultra-low-power and neuron-inspired analog-to-digital conversion for biomedical system. **(9)**

LOW-POWER BIOMEDICAL SYSTEMS

Wireless inductive power links for medical implants - Energy-harvesting RF antenna power links - Low-power RF telemetry in biomedical implants - Ultra-low-power implantable medical electronics- cochlear implants or bionic ears - an ultra-low power programmable analog bionic ear processor - low power electrode stimulation - highly miniature electrode - stimulation. **(8)**

BIOMEDICAL ELECTRONIC SYSTEMS

Brain machine interfaces for the blind - Brain machine interface for paralysis, speech, and other disorders. Ultra-low-power non-invasive medical electronics - switched-capacitor model of the heart - micro-power electrocardiogram amplifier - Low-power pulse oximetry - Battery-free tags for body sensor networks - Intra-body galvanic communication networks - Biomolecular sensing. **(9)**

PRINCIPLES FOR ULTRA-LOW-POWER ANALOG AND DIGITAL DESIGN

Digital design: Sizing and topologies for robust subthreshold operation - power dissipation - energy efficiency Optimization - Varying power supply voltage and threshold voltage - gated clocks - Basics of adiabatic computing - Architectures and algorithms for improving energy efficiency.

Analog and mixed-signal design: Power consumption in analog and digital systems - optimum point for digitization in a mixed-signal system - The Shannon limit for energy efficiency - Collective analog or hybrid computation - HSMs: general-purpose mixed-signal systems with feedback - General principles for low-power mixed-signal system design - Actuators and sensors. **(10)**

BIO-INSPIRED SYSTEMS

Neuromorphic electronics - RF-cochlea design - bio-inspired analog vocal tract - vision architectures - Spike-based hybrid computers - Energy efficiency Cytomorphic electronics: cell-inspired electronics - Electronic analogies of chemical reactions - Log-domain current-mode models of chemical reactions and protein-protein networks - Analog circuit models of gene-protein dynamics - gene-protein circuits - Hybrid analog-digital computation in cells, neurons and brain. **(9)**

TOTAL : 45

REFERENCES

1. *Rahul Sarpeshkar, "Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems", Cambridge University Press, 2011.*
2. *Kris Iniewski, "VLSI Circuit Design for Biomedical Applications", Artech House Publishers, 2008.*
3. *Tan Nianxiong Nick, Li Dongmei, Wang Zhihua, "Ultra Low Power Integrated Circuit Design: Circuits, Systems, and Applications", Springer Publications, 2014.*
4. *A. Mead, "Analog VLSI and Neural Systems", Addison Wesley Publishing Company, 1990.*
5. *Lee," The Design of CMOS Radio-Frequency Integrated Circuits", 2nd Edition, Tata McGraw Hill, 2004.*

15MVDE14 - GENETIC ALGORITHMS FOR VLSI

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on concept of genetic algorithms and its usage for partitioning, placement, FPGA mapping, testing and power estimation for optimal VLSI circuits.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *apply genetic algorithm to various stages of VLSI design such as floor planning, partitioning and placement*

CO2 : *generate optimal vectors for testing, FPGA mapping, automatic test generation and power estimation using genetic algorithm and comparing its performance with conventional algorithms.*

OVERVIEW OF GENETIC ALGORITHMS

Introduction to GA Technology - Simple GA algorithm -Steady State Algorithm - Selection - Crossover - Mutation - Fitness Scaling - Inversion. **(9)**

GENETIC ALGORITHM FOR VLSI DESIGN

GA for VLSI Design, Layout and Test automation - Partitioning - Automatic Placement - Automatic Routing - Technology mapping for FPGAs - Automatic test generation - Genetic Multiway Partitioning **(9)**

ADVANCED GENETIC ALGORITHMS

Hybrid genetic - Genetic encoding - Local improvement - WDFR - Comparison of CAs - Standard cell placement - GASP algorithm - Unified algorithm. **(9)**

GENETIC ALGORITHM FOR VLSI TESTING

Macro Cell Global routing - FPGA technology mapping - Circuit segmentation - Test generation in a GA frame work - Test generation procedures. **(9)**

APPLICATIONS

Power estimation - Application of GA - Standard cell placement - GA for ATG - Problem Encoding - Fitness function - GA vs Conventional Algorithm. **(9)**

TOTAL : 45

REFERENCES

1. *Pinaki Mazumder, E.MRudnick, "Genetic Algorithm for VLSI Design, Layout and test Automation", Prentice Hall, 1999*
2. *Randy L. Haupt, Sue Ellen Haupt, "Practical Genetic Algorithms" Second Edition, John Wiley & Sons, 2004*
3. *Ricardo Sal Zebulum, Macro Aurelio Pacheco, Marley Maria B.R. Vellasco, Marley Maria Bernard Vellasco "Evolution Electronics: Automatic Design of electronic Circuits and Systems Genetic Algorithms", CRC press, 2001.*
4. *M.J.S .Smith, "Application Specific Integrated Circuits", Addison -Wesley, 1997*
5. *John R.Koza, Forrest H.Bennett, David Andre, Morgan Kufmann, "Genetic Programming: Automatic Discovery of Reusable Programs", MIT Press, 1999.*

15MVDE15 - NETWORK ON CHIP

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on fundamentals of 3D Network-on-chip, security, verification and monitoring of NoC, Types and architecture of routers for NoC, routers for 3D architecture

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 *: explain the need for 3D NOC, concepts used in testing and fault tolerance*

CO2 *: describe the energy and power issues, architecture and working of routers in 3D NOC*

INTRODUCTION TO THREE DIMENSIONAL NOC

Three-Dimensional Networks-on-Chips - Architectures - Resource Allocation for QoS - On-Chip Communication - Networks-on-Chip - Protocols-On-Chip Processor Traffic Modeling for Networks-on-Chip. **(9)**

TEST AND FAULT TOLERANCE OF NOC

Design - Security in Networks-on-Chips - Formal Verification of Communications in Networks-on-Chips - Test and Fault Tolerance for Networks-on-Chip Infrastructures - Monitoring Services for Networks-on-Chips. **(9)**

ENERGY AND POWER ISSUES OF NOC

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips **(9)**

MICRO-ARCHITECTURE OF NOC ROUTER

Baseline NoC Architecture - MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers - RoCo: The Row-Column Decoupled Router - A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures. **(9)**

DIMDE ROUTER FOR 3D NOC

A Novel Dimensionally - Decomposed Router for On-Chip Communication in 3D Architectures - Digest of Additional NoC MACRO - Architectural Research. **(9)**

TOTAL : 45

REFERENCES

1. *Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita.R.Das, "Networks-on-Chip Architectures: A Holistic Design Exploration", Springer, 2009.*
2. *Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi, "Networks-on-Chips: Theory and Practice", CRC press, 2009.*
3. *Axel Jantsch, Hannu Tenhunen, "Networks on Chip", Springer, 2003.*
4. *Giovanni De Micheli, Luca Benini, "Networks on Chips: Technology and Tools (Systems on Silicon)", Morgan Kaufmann, 2006.*
5. *Jose Flich , Davide Bertozzi, "Designing Network On-Chip Architectures in the Nanoscale Era", CRC Press, 2010.*

15MVDE16 - HARDWARE SOFTWARE CO-DESIGN

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will acquire knowledge on various design steps in hardware/software co-design environment and will experience process optimization while considering various design decisions using contemporary high-level methods and tools.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain the concepts of hardware and software co-design and its methodologies.*

CO2 : *integrate hardware and software, incorporate OOPs concept in hardware design and write system C program for practical competence.*

SYSTEM SPECIFICATION AND MODELLING

Embedded Systems - Hardware/Software Co-Design - Co-Design for System Specification and Modelling - Co-Design for Heterogeneous Implementation - Processor Synthesis - Single-Processor Architectures with one ASIC - Single-Processor Architectures with many ASICs- Multi-Processor Architectures - Comparison of Co-Design Approaches - Models of Computation-Requirements for Embedded System Specification. **(9)**

HARDWARE/SOFTWARE PARTITIONING

The Hardware/Software Partitioning Problem- Hardware-Software Cost Estimation-Generation of the Partitioning Graph - Formulation of the HW/SW Partitioning Problem - Optimization - HW/SW Partitioning based on Heuristic Scheduling- HW/SW Partitioning based on Genetic Algorithms. **(9)**

HARDWARE-SOFTWARE INTEGRATION

Prototyping and Emulation Techniques-Target Architectures-Micro programmed Architectures-General-Purpose Embedded Cores- System-on-Chip - Hardware-Software Interfaces - Principles of Hardware/ Software Communication- Microprocessor Interfaces- Hardware Interfaces. **(9)**

OBJECTED ORIENTED HARDWARE DESIGN

Motivation for object oriented techniques- object oriented design strategies - modelling hardware components as classes- designing specialized components- data decomposition- Processor example. **(9)**

SYSTEM C PROGRAMMING

Design Methodology - Modules and Hierarchy- Processes- Ports and signals- Data types- Simulation using SystemC. Case Study: Processor/Coprocessor design using System C. **(9)**

TOTAL : 45

REFERENCES

1. *Patrick Schaumont, "A Practical Introduction to Hardware/Software Co-design", Patrick Schaumont, 2nd Edition, Springer, 2012.*
2. *Ralf Niemann, "Hardware/Software Co-Design for Data Flow Dominated Embedded Systems", Kluwer Academic Publishers, 1998.*
3. *Alxel Jantsch,"Modelling Embedded Systems and SOC's. Concurrency and Time in Models of Computation", Morgan Kaufmann Publishers, 2004.*
4. *Vahid, Frank, "Embedded system design : A Unified Hardware / Software Introduction", Wiley, 2002.*
5. *Berger A S, "Embedded Systems Design. An Introduction to Processes, Tools, & Techniques", CMP Books, 2002.*
6. *Sanjay Kumar, "The Codesign of Embedded Systems: A Unified Hardware / Software Representation", Kluwer Academic Publishers, 1995.*
7. *Grotker T., Liao S., Martin G and Swan S, "System design with System C", Kluwer Academic Publishers, 2002.*

15MVDE17 - VLSI FOR WIRELESS COMMUNICATION

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on Modulation techniques, Spread Spectrum, Receiver Architecture, Low Noise Amplifier, Analog to Digital Converters & Synthesizer and VLSI architecture for Wireless Systems,

COURSE OUTCOME

Upon the completion of the course, students will be able to demonstrate ability to

CO1 : *narrate different Modulation techniques, Spread Spectrum and Receiver Architecture*

CO2 : *analyze the concepts of Low Noise Amplifier, Analog to Digital Converters & Synthesizer and VLSI architecture for Wireless Systems.*

INTRODUCTION

Review of Modulation Schemes - BFSK- BPSK -QPSK - OQPSK - Classical Channel - Additive White Gaussian Noise - Finite Channel Bandwidth - Wireless Channel - Path Environment - Path Loss - Friis Equation - Multipath Fading - Channel Model - Envelope Fading - Frequency Selective Fading - Fast Fading - Comparison of different types of Fading- Review of Spread Spectrum - DSSS - FHSS - Principle of DSSS - Modulation - Demodulation - Performance in the presence of noise - narrowband and wideband interferences. **(9)**

RECEIVER ARCHITECTURE

Receiver Front End - Motivations - General Design Philosophy- Heterodyne and Other architectures - Filter Design - Band Selection Filter - Image Rejection Filter - Channel Filter - Non idealities and Design Parameters - Harmonic Distortion - Intermodulation - Cascaded Nonlinear Stages - Gain Compression - Blocking - Noise - Noise Sources - Noise Figure - Design of Front end parameter for DECT. **(9)**

LOW NOISE AMPLIFIER

Low Noise Amplifier - Matching Networks - Matching for Noise and Stability - Matching for Power - Implementation - Comparison of Narrowband and Wideband LNA - Wideband LNA Design - Narrowband LNA - Impedance matching -Power matching- Salient features of LNA -Core Amplifier Design. **(9)**

ANALOG TO DIGITAL CONVERTERS & SYNTHESIZER

Demodulators - Delta Modulators - Low Pass Sigma Delta Modulators - High Order Modulators - One Bit DAC and ADC -Passive Low Pass Sigma Delta Modulator - Band pass Sigma Delta Modulators - Comparison - PLL based Frequency Synthesizer. **(9)**

VLSI ARCHITECTURE FOR WIRELESS SYSTEMS

Implementations: VLSI architecture for Multi-tier Wireless System - Hardware Design Issues for a Next generation CDMA System - Efficient VLSI Architecture for Base Band Signal processing. **(9)**

TOTAL : 45

REFERENCES

1. *Bosco Leung, "VLSI for wireless Communication", Springer, 2nd Edition, 2011.*
2. *Andreas F.Molisch, "Wideband wireless Digital Communication", Prentice Hall PTR, 2001.*
3. *George.V.Tsoulous, "Adaptive Antennas for wireless Communication", IEEE Press, Willey Publications, 2001.*
4. *Xiaodong Wang and H.Vincent Poor, "Wireless Communication System ,Advanced Techniques for Signal Reception", Pearson Education. 2004.*
5. *Wolfgang Eberle, "Wireless Transceiver Systems Design", Springer, 2008.*

15MVDE18 - VLSI SIGNAL PROCESSING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on DSP algorithms, retiming techniques, unfolding and folding algorithms, systolic architectures, fast convolution algorithms, pipelining and parallel processing of IIR and adaptive filters, algorithmic and numerical strength reduction techniques.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *apply iteration bound to data flow graphs, analyze pipelining and parallel processing of FIR filters, examine retiming and design systolic architectures.*

CO2 : *design architectures for convolution algorithms, IIR and adaptive filters and explain about algorithmic and numerical strength reduction techniques.*

DIGITAL SIGNAL PROCESSING SYSTEMS

Introduction to DSP Processors and Systems - Typical DSP algorithms - data flow graph representations - loop bound and iteration bound - Longest Path Matrix algorithm - Pipelining and parallel processing - Pipelining of FIR digital filters - parallel processing - pipelining and parallel processing for low power - Retiming - definitions and properties - retiming techniques. **(9)**

UNFOLDING, FOLDING AND SYSTOLIC ARCHITECTURES

Unfolding Algorithm - Properties and Applications of Unfolding - Folding Transformation - Systolic Array design - FIR systolic arrays - Selection of Scheduling Vectors - Matrix multiplication and 2D systolic array design. **(9)**

FAST CONVOLUTION AND ALGORITHMIC STRENGTH REDUCTION

Cook-Toom Algorithm - Inefficient/Efficient Single Channel Interleaving - Cyclic convolution - Algorithmic strength reduction in FIR filters and DCT - Look-Ahead pipelining in first-order IIR filters - parallel processing of IIR filters - combined pipelining and parallel processing for IIR filters - pipelined adaptive digital filters. **(9)**

BITLEVEL ARIHTMETIC ARCHITECTURES

Scaling and Round-off Noise - Computation - Round-off Noise in Pipelined first-order IIR Filters - Bit-Level Arithmetic Architectures: Parallel Multipliers with sign extension - Parallel Carry-Ripple Array Multipliers - Parallel Carry-Save Array Multiplier - 4x4 bit Baugh-Wooley Carry-Save Multiplier - Bit-Serial FIR Filter Design and Implementation. **(9)**

NUMERICAL STRENGTH REDUCTION

Numerical Strength Reduction - Subexpression Elimination - Multiple Constant Multiplication - Iterative Matching - Linear Transformations - Synchronous, Wave and Asynchronous Pipelining - Synchronous

Pipelining and Clocking Styles - Clock Skew and Clock Distribution in bit-level Pipelined VLSI Designs - Wave Pipelining - Asynchronous Pipelining. **(9)**

TOTAL : 45

REFERENCES

1. *Keshab K.Parhi, "VLSI Digital Signal Processing Systems, Design and implementation", Wiley, Interscience, 1999.*
2. *U.Meyer Baese , "Digital Signal Processing with Field Programmable Arrays", Springer, 2007.*
3. *Mohammed Ismail and Terri Fiez, "Analog VLSI Signal and Information Processing", McGraw Hill, 1994.*
4. *S.Y. Kung, H.J. White House, T. Kailath, "VLSI and Modern Signal Processing", Prentice Hall, 1985.*
5. *Jose E. France, Yannis Tsividis, "Design of Analog, Digital VLSI Circuits for Telecommunication and Signal Processing", Prentice Hall, 1994.*
6. *Behrooz Parhami, "Computer Arithmetic: Algorithms & Hardware Designs", Oxford University Press, 2nd Edition, 2010.*

15MVDE19 - VLSI ARCHITECTURE FOR IMAGE AND VIDEO PROCESSING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on image and video processing algorithms and design VLSI architectures.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *analyze various architectures to realize Image processing algorithms and explain the 3D image processing algorithms*

CO2 : *explore various processing techniques of Image and Video signals and design different architectures for Image and Video signal processing.*

IMAGE PROCESSING ALGORITHMS AND ARCHITECTURES

Image Processing Tasks - Low level Image Processing Operations - intermediate level operations Image processor architecture: Requirements and Classification - Uni and Multi processors - MIMD systems - SIMD systems - Pipelines - Design aspects of real time low level image processors - Design method for special architectures. **(9)**

3D IMAGE PROCESSING

Overview of 3D image - Types and characteristics of 3D image processing - Examples of 3D image processing, Continuous and digitized images, Models of image operations, Algorithm of image operations - Smoothing filter - Difference filter - Differential features of a curved surface - Region growing. **(9)**

PIPELINED, 2D AND 3D IMAGE PROCESSING ARCHITECTURES

Architecture of a cellular logic processing element - Second decomposition in data path and control - Real time pipeline for low level image processing - Design aspects of Image Processing architectures - Implementation of Low level 2D and 3D and Intermediate level algorithms. **(9)**

VIDEO PROCESSING ALGORITHMS

Introduction to Video Processing, Video Sampling and Interpolation, Motion Detection and Estimation Algorithms, Video Enhancement and Restoration, Video Stabilization and Mosaicing-Video Segmentation - MPEG-4 Visual and Fast Motion Estimation Algorithms. **(9)**

VIDEO PROCESSING ARCHITECTURES

General design space evaluation - Design space motion estimation architectures - Motion estimation architectures for MPEG-4 - Design Trade offs - VLSI Implementation search engine I and Search engine II. **(9)**

TOTAL : 45

REFERENCES

1. *Peter M. Kuhn, "Algorithms, Complexity Analysis and VLSI Architectures for MPEG-4 Motion Estimation", Springer, 2010.*
2. *Pieter Jonker, "Morphological Image Processing: Architecture and VLSI design", Springer, First Edition, 1992.*
3. *Sid Ahmed M.A., "Image Processing - Theory, Algorithm and Architectures", McGraw Hill, 2009.*
4. *A.MuratTekalp, "Digital Video Processing", Pearson Education, Noida, 2010.*
5. *Junichiro Toriwaki · Hiroyuki Yoshida, "Fundamentals of Three-Dimensional Digital Image Processing", Springer 2009.*
6. *Alan C. Bovik, "The Essential Guide to Video Processing", Academic Press, 2009.*
7. *King-sun Fu, "VLSI for Pattern Recognition and Image Processing", Springer-Verlag, 1984.*

15MVDE20 - RECONFIGURABLE ARCHITECTURES

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on fundamentals of reconfigurable architectures, classification of FPGA based on the basic blocks, application specific design styles, Routing of FPGA, Technology independent optimization, high level synthesis and RCS for specific applications.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate ability to

CO1 : *report on the reconfigurable architecture and FPGA fundamentals.*

CO2 : *explain the routing process and describe the optimization techniques for technology independent designs and use of RCAs in ASIC design.*

INTRODUCTION

Domain - specific processors - Application specific processors - Reconfigurable Computing Systems - Evolution of Reconfigurable systems - Characteristics of RCS advantages and issues - Fundamental concepts and design steps - Classification of reconfigurable architecture - fine, coarse, grain & hybrid architectures - examples **(9)**

FPGA TECHNOLOGIES AND ARCHITECTURE

Technology trends - Programming Technology - SRAM programmed FPGAs - anti-fuse Programmed FPGA's - Erasable programming logic devices - Alternative FPGA architectures: MUX vs LUT based logic blocks - CLB vs Slices - fast carry chains - Embedded RAM - FPGA vs ASIC Design styles. **(9)**

ROUTING FOR FPGAS

General strategy for touting in FPGAS - Routing for row based FPGAS - Segmented channel routing - definitions - Algorithm for I segment and K segment routing - Routing for symmetrical FPGAs - flexibility of FPGA Routing Architectures - FPGA architectural assumption - Logic Block, connection block - switch block - Effect of connection block flexibility on Routability - Effect of switch block flexibility on Routability - Tradeoffs in flexibility of S and C blocks. **(9)**

HIGH LEVEL DESIGN

FPGA design style: Technology independent optimization - Technology mapping - Placement. High level synthesis of reconfigurable hardware - high - level languages - design tools - Simulation of cycle based and event driven based - Synthesis logic - HDL Vs Physically aware- timing analysis - static Vs dynamic - Verification physical design tools. **(9)**

APPLICATION SPECIFIC RCS

Efficient architectures - power efficient architectures - low energy reconfigurable single chip DSP system - minimizing the memory requirement for condition flow FFT implementation - memory reduction methods for FFT implementation - RCS for embedded cores, image processing. **(9)**

TOTAL : 45

REFERENCES

1. *Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer, 2007.*
2. *Clive Max Maxfield, "The Design Warriors Guide to FPGAs: Devices, Tools and Flows, Newnes", Elsevier, 2006.*
3. *Jorgen Staunstrup, Wayne Wolf, "Hardware / software Co - Design: Principles and Practice", Kluwer Academic Publishers, 1997.*
4. *Stephen D.Boren, Robert J. Francis, Jonathan Rose, Zvonko G. Vranesic, "Field Programmable Gate Array", Kluwer Academic Publishers, 1992.*
5. *Yuke Wang, Yiyan Tang, Yingtao Jiang, Jin-Gym Chung , "Novel Memory Reference Reduction Methods for FFT Implementations on DSP Processors", IEEE transactions on Signal Processing , Vol.55, No.5, pp. 2338-2349, May 2007.*
6. *Russell Tessier and Wayne Burleson, "Reconfigurable computing for Digital Signal Processing: A Survey", Journal of VLSI Signal Processing, Vol.28, pp.7-27, 2001.*

15MVDE21 - SYSTEM ON CHIP

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of ME VLSI Design will be able to acquire knowledge on fundamentals and concepts of SoC, designing various components on SoC and its challenges, methods of validating the correctness of the design and testing methodologies.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain the concepts of SoC and the design criteria for the logic core.*

CO2 : *design memory and analog cores, illustrate the correctness of the design using various verification and testing methodologies.*

INTRODUCTION

System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology - SoC design issues - SoC challenges and components. **(9)**

DESIGN METHODOLOGICAL FOR LOGIC CORES

SoC Design Flow - On-chip buses - Design process for hard cores - Soft and firm cores - Designing with hard cores and soft cores - Core and SoC design examples. **(9)**

DESIGN METHODOLOGY FOR MEMORY AND ANALOG CORES

Embedded memories - Simulation modes - Specification of analog circuits - A/D converter - Phase-located loops - High I/O. **(9)**

DESIGN VALIDATION

Core level validation -Test benches - SoC design validation - Co simulation - hardware/ Software co-verification. Case Study: Validation and test of systems on chip. **(9)**

SOC TESTING

SoC Test Issues - Testing of digital logic cores - Cores with boundary scan - Test methodology for design reuse - Testing of microprocessor cores - Built in self test method - testing of embedded memories. Case Study: Integrating BIST techniques for on-line SoC testing. **(9)**

TOTAL : 45

REFERENCES

1. *Rochit Rajsunah, "System-on-a-chip: Design and Test", Artech House, 2007.*
2. *Prakash Raslinkar, Peter Paterson & Leena Singh, "System-on-a-chip verification: Methodology and Techniques", Kluwer Academic Publishers, 2000.*
3. *M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, "Low Power Methodology Manual for System-on-Chip Design Series: Integrated Circuits and Systems", Springer, 2007.*
4. *A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, "Integrating BIST techniques for on-line SoC testing, IEEE Symposium on On-Line Testing, 2005.*
5. *Ricardo Rels, "Design of System on Chip: Devices and Components" Springer, July 2004.*

15MVDE22 - PHYSICAL DESIGN OF VLSI CIRCUITS

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of ME VLSI Design will be able to acquire knowledge on fundamentals of VLSI technology, Rules of layout, partitioning, floor planning, placement and routing algorithms, delays in gates and interconnects, single layer& multichip module routing and compaction techniques.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 : *explain the concepts of partitioning, floor planning, placement and routing of the cells as per the layout rules using the top down approach.*

CO2 : *report on delay modeling, delay minimization, examine single layer and over the cell routing and apply 1D and 2D compaction techniques.*

INTRODUCTION TO VLSI TECHNOLOGY

Layout Rules - Circuit abstraction Cell generation using programmable logic array transistor chaining - Wein Berger arrays and gate matrices - layout of standard cells gate arrays and sea of gates - Field Programmable Gate Array (FPGA) - layout methodologies Packaging - Computational Complexity - Algorithmic Paradigms. **(9)**

PLACEMENT USING TOP-DOWN APPROACH

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan - Lin Heuristic Ratio cut partition with capacity and I/O constraints. Floor planning: Rectangular dual floor planning hierarchical approach - simulated annealing - Floor plan sizing. Placement: Cost function - force directed method - placement by simulated annealing partitioning placement - module placement on a resistive network - regular placement linear placement. **(9)**

ROUTING USING TOP DOWN APPROACH

Fundamentals: Maze Running - line searching- Steiner trees Global Routing: Sequential Approaches - hierarchical approaches - multi commodity flow based techniques - Randomized Routing - One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA - Row based FPGAs. **(9)**

PERFORMANCE ISSUES IN CIRCUIT LAYOUT

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing - Driven Placement: Zero Stack Algorithm- Weight based placement - Linear Programming Approach Timing riving Routing: Delay Minimization- Click Skew Problem - Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization. **(9)**

SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION

Planar subset problem (PSP) - Single Layer Global Routing - Single Layer detailed Routing - Wire length and bend minimization technique - Over The Cell (OTC) Routing Multiple chip modules (MCM) - programmable Logic Arrays - Transistor chaining - Wein Burger Arrays - Gate matrix layout - 1D compaction - 2D compaction. **(9)**

TOTAL : 45

REFERENCES

1. *Majid Sarrafzadeh, C. K. Wong, "An Introduction to VLSI Physical Design", McGraw Hill, 1996.*
2. *Preas M. Lorenzatti, "Physical Design and Automation of VLSI systems", The Benjamin Cummins Publishers, 1998.*
3. *Sadiq M. Sait, ?Habib Youssef, "VLSI Physical Design Automation: Theory and Practice", World Scientific Publishers, 1999.*
4. *Sung Kyu Lim, "Practical Problems in VLSI Physical Design Automation", Springer Publications, 2008.*
5. *Andrew B. Kahng, Jens Lienig, Igor L. Markov, Jin Hu , "VLSI Physical Design: From Graph Partitioning to Timing Closure", Springer Publications, 2011.*
6. *John P. Uyemura, "Introduction to VLSI Circuits and Systems", John Wiley and Sons, 2002*

15MVDE23 - ARTIFICIAL INTELLIGENCE AND OPTIMIZATION TECHNIQUES

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on computational methods inspired by nature, such as neural networks, genetic algorithms, ant colony and particle swarm optimization, artificial immune systems, cellular automata, and multi-agent systems and adopt these techniques to solve problems in the real world applications.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 *: explain the concepts of nature inspired techniques like neural networks and fuzzy logic systems, and apply them to real world problems.*

CO2 *: describe about and genetic algorithms, ant colony and swarm optimization algorithms and apply them to solve problems in classification, pattern recognition, prediction, rule extraction, and optimization problems.*

NEURAL NETWORKS

Basic concepts - single layer perceptron - Multi layer perceptron - Adaline - Madaline - Learning rules- Supervised learning - Back propagation networks - Training algorithm - Practical difficulties - Advanced algorithms - Adaptive network - Radial basis network - modular network - Applications. **(9)**

FUZZY LOGIC SYSTEMS

Basic of fuzzy logic theory - crisp and fuzzy sets - Basic set operation like union - interaction - complement - T-norm - T-conorm - Composition of fuzzy relations - fuzzy if-then rules - Fuzzy reasoning - Neuro-Fuzzy Modeling: Adaptive Neuro-Fuzzy Inference System (ANFIS), ANFIS architecture - Hybrid Learning Algorithm. **(9)**

GENETIC ALGORITHMS

Fundamentals of genetic algorithm - Mathematical foundations - Genetic modeling - Survival of the fittest crossover - Inversion and Deletion - mutation - reproduction - Generational cycle -rank method - rank space method - Other derivative free optimization - simulated annealing, Random search, Downhill simplex search - Application. **(9)**

ANT COLONY OPTIMIZATION

Ant Colony Optimization: Introduction - From real to artificial ants - Theoretical considerations - Convergence proofs - ACO Algorithm - ACO and model based search - Application principles. **(9)**

SWARM OPTIMIZATION

Particle Swarm Optimization: Introduction, Principles of bird flocking and fish schooling - Evolution of PSO - Operating principles - PSO Algorithm - Neighborhood Topologies - Convergence criteria - Applications of PSO - Honey Bee Social Foraging Algorithms - Bacterial Foraging Optimization Algorithm. **(9)**

TOTAL : 45

REFERENCES

1. *Laurene Fauseett, "Fundamentals of Neural Networks", Prentice Hall, 1994.*
2. *Jyh-Shing Roger Jang, Chuen-Tsai Sun, Eiji Mizutani, "Neuro-fuzzy and Soft Computing: A Computational Approach to Learning and Machine Intelligence", Prentice Hall, 1997.*
3. *Timothy J.Ross, "Fuzzy Logic Engineering Applications", Mc-Graw Hill, New York, 2004.*
4. *David E.Goldberg, "Genetic Algorithms in Search, Optimization, and Machine Learning", Pearson Education, Asia, 1996.*
5. *Marco Dorigo and Thomas Stutzle, "Ant Colony optimization", Prentice Hall, New Delhi, 2004.*
6. *N P Padhy, "Artificial Intelligence and Intelligent Systems", Oxford University Press, 2005.*

15MVDE24 - RELIABILITY ENGINEERING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will be able to acquire knowledge on Probability Plotting , Load-Strength Interference, reliability prediction, concepts of reliability and durability, reliability and testing of electronic components and the process of manufacturing and reliability management.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 *: explain the basic concepts of probability plotting and Load-Strength Interference, describe the concepts of reliability, modeling and design of electronic components.*

CO2 *: report on the concepts of reliability and durability and manage reliability.*

PROBABILITY PLOTTING AND LOAD-STRENGTH INTERFERENCE

Statistical distribution - Statistical confidence and hypothesis testing - Probability plotting techniques - Weibull - Extreme value - Hazard - binomial data - Analysis of Load - Strength interference - Safety margin and loading roughness on reliability. **(9)**

RELIABILITY PREDICTION - MODELLING AND DESIGN

Statistical design of experiments and analysis of variance Taguchi method - Reliability prediction - Reliability modelling - Block diagram and Fault tree Analysis - Petric Nets - State space Analysis - Monte Carlo simulation - Design analysis methods - quality function deployment - load strength analysis - failure modes - effects and criticality analysis. **(9)**

ELECTRONICS AND SOFTWARE SYSTEMS RELIABILITY

Reliability of electronic components - component types and failure mechanisms - Electronic system reliability prediction - Reliability in electronic system design - software errors - software structure and modularity - fault tolerance - software reliability - prediction and measurement - hardware/software interfaces **(9)**

RELIABILITY TESTING AND ANALYSIS

Test environments - testing for reliability and durability - failure reporting - Pareto analysis - Accelerated test data analysis - CUSUM charts - Exploratory data analysis and proportional hazards modeling - reliability demonstration - reliability growth monitoring **(9)**

MANUFACTURE AND RELIABILITY MANAGEMENT

Control of production variability - Acceptance sampling - Quality control and stress screening - Production failure reporting - preventive maintenance strategy - Maintenance schedules - Design for maintainability - Integrated reliability programmes - reliability and costs - standard for reliability - quality and safety - specifying reliability - organization for reliability. **(9)**

TOTAL : 45

REFERENCES

1. *Patrick D.T. O'Connor, David Newton and Richard Bromley, "Practical Reliability Engineering", 4th Edition, John Wiley & Sons, 2002.*
2. *David J. Klinger, Yoshinao Nakada, Maria A. Menendez and Van Nostrand-Reinhold, "AT & T Reliability Manual", 5th Edition, Springer, 1998.*
3. *Gregg K. Hobbs, "Accelerated Reliability Engineering - HALT and HASS", John Wiley & Sons, New York, 2000.*
4. *Lewis, "Introduction to Reliability Engineering", 2nd Edition, Wiley International 1996*

15MVDE25 - PATTERN RECOGNITION AND MACHINE LEARNING

L	T	P	C
3	0	0	3

ASSESSMENT : THEORY

COURSE OBJECTIVE

The students of M.E VLSI Design will acquire knowledge on statistical pattern recognition, machine learning and design of different artificial intelligence models, state-of-art algorithms used in machine learning and optimization methods.

COURSE OUTCOME

Upon completion of the course, students will be able to demonstrate an ability to

CO1 *: design feature recognition systems tailored for specific applications using artificial neural networks.*

CO2 *: design artificial intelligence models and develop classifiers and machine learning systems using state-of-art algorithms and optimization methods.*

INTRODUCTION

Definition of learning systems - Goals and applications of machine learning - Aspects of developing a learning system- training data - concept representation - Function approximation. **(9)**

ARTIFICIAL NEURAL NETWORKS

Neurons and biological motivation - Linear threshold units - Perceptrons - representational limitation and gradient descent training - Multilayer networks and back propagation - Hidden layers and constructing intermediate - distributed representations. **(9)**

ARTIFICIAL INTELLIGENCE MODELS

Linear models: polynomial regression - over-fitting - model selection - logistic regression - Naive Bayes - Non-linear models: decision trees - instance-based learning- neural networks - Support Vector Machines: Maximum margin linear separators - Quadratic programming solution - maximum margin separators- Kernels for learning non-linear functions. **(9)**

GAME THEORY

Fundamentals - Conflict - Strategy and Games - Game theory - The Prisoner's Dilemma - Games in normal and extensive forms - Representation - Examination - Examples. **(9)**

OPTIMIZATION METHODS

Heuristic and Meta - heuristic search techniques - stochastic search methods - social algorithms: ant colony, artificial bee colony, particle swarm optimization - applications. **(9)**

TOTAL : 45

REFERENCES

1. *Christopher Bishop, "Pattern Recognition and Machine Learning", Springer, 2006.*
2. *Richard Duda, Peter Hart and David Stork, "Pattern Classification", 2nd Edition, Wiley, 2001.*
3. *Tom Mitchell, "Machine Learning", McGraw-Hill, 1997.*
4. *Russel, S.J. and Norvig, P., "Artificial Intelligence a Modern Approach", 2nd Edition, New Jersey, Prentice Hall, 2002*
5. *Rich, E. and Knight, K. "Artificial Intelligence", 2nd Edition, New York: McGraw-Hill, 1991.*
6. *E. N. Barron, "Game Theory: An Introduction", Wiley, 2009.*
7. *Rajiv J. Kapadia, "Optimisation in Signal and Image Processing", John Wiley & Sons, 2010.*

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(1956 - 2016)

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

M.E. VLSI DESIGN

CURRICULUM AND SYLLABI

UNDER CHOICE BASED CREDIT SYSTEM

(For the students admitted during the academic year 2015-2016 and onwards)

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